Benchtop linear power supply: design, construction and characterisation

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Abstract

This document describes the design, simulation and characterisation of a general purpose benchtop linear power supply that incorporates current limiting. This is work in progress, results are documented as they are obtained.

1 LPS characteristics, features and design goals

Ultimately, a general purpose power supply performs a single function; provide a constant voltage to a load irrespective of any time dependent current requirement. All power supplies exhibit nonideal behaviour. The following are commonly specified to describe power supply quality,

- Noise and ripple
- Load regulation
- Transient response

Noise and ripple

The magnitude of noise and ripple present on the output of a linear power supply indicates how far the supply is from ideally regulated. A low-noise/ripple supply may be important for powering certain classes of circuits. For example, relatively small amounts of supply noise may adversely effect the performance of precision spectral analysis circuits.

Load regulation

Load regulation indicates the degree of dependence that the output voltage has on the static load current and is defined by the equation,

$$\% \text{ Load regulation} = 100\% \frac{\Delta V_{\text{out}}}{\Delta I_{\text{load}}} \frac{1}{V_{\text{out}}} \tag{1}$$

Transient response

Sudden changes in load current result in transient fluctuations of the supply voltage. When designing a power supply great attention must be given to its transient behaviour. Transient behaviour indicates the degree of stability of the power supply, which must be ensured for all expected load conditions. In addition, excessive ringing of the output voltage in response to sudden changes of load current can be considered as load induced noise.

Power supply features

A general purpose benchtop power supply must have two supplies at a minimum to allow for the powering of split-rail analog circuits. The addition of a third, lower voltage supply is useful for powering mixed analog and digital circuits. Current limiting is vital for R&D purposes to (hopefully) eliminate the possibility of circuit destruction. A constant current mode has many applications beyond circuit protection. Digitally controlling and monitoring the power supply voltage, load current and current limit enhances its functionality. For example, microcontroller routines can be written for battery charging applications or circuit and component I-V characterisation.

The upper supply voltage and current capability must be chosen. Increasing the voltage and current capability extends the usability of the supply, all-be-it with diminishing returns. However, an increase of the voltage capability comes with increasing costs of thermal dissipation management and transformer size. An upper voltage of about 35 V and a continuous current capability of 4 A are tentatively chosen. A tentative list of the power supply features include:

- Two independent and electrically isolated voltage adjustable channels with a 35V and 4A capability.
- A third lower-voltage adjustable channel intended for the powering of digital circuits, also electrically isolated.
- Analog constant current and digital shutdown protection modes on all channels.
- Digital control of voltage and current limit.
- Load current and voltage readout.
- Computer USB interface for data logging.

A single control board shall communicate with the 3 power boards and handle all user interface and data logging tasks. A description of the third, lower voltage supply will be given after that of the main supplies.

2 Power board analog design

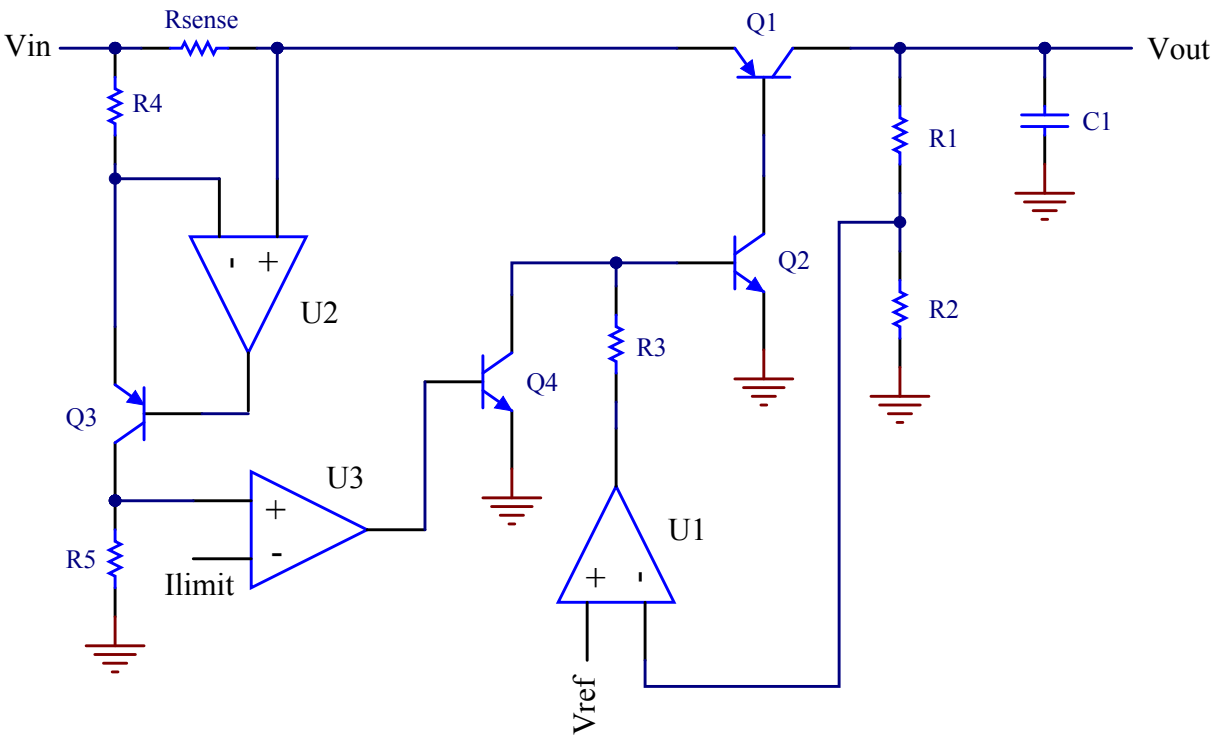

Figure 1: Basic topology of the constant voltage and constant current control loops.

The proposed topology of the constant voltage (CV) and constant current (CC) control loops is shown in figure 1. Opamps are an ideal choice for central use in the control loops since low cost and high performance options are available.

Opamp requirements

Noise

The wide band output voltage noise of the CV loop is ultimately limited by the input noise of the opamp, U1 (of figure 1). Reference voltage noise and thermal noise of the feedback resistors (R1 and R2) also contribute to the voltage noise. Reference voltage noise can be filtered, although, filtering low-frequency noise might be cumbersome. Within the frequency band 10 Hz-100 kHz a total output noise voltage of 50 μV_{RMS} is a low noise figure for a linear power supply and is chosen as the maximum specification limit. If noise is dominated by the opamp voltage noise its density, $\mathrm{e_n}$, must be less than,

$$\mathrm{e_n} < \frac{50\,\mu V}{\sqrt{10^5 - 10}} \frac{R2}{R1 + R2} = \frac{R2}{R1 + R2} \times 158\,nV_{\mathrm{RMS}}/\sqrt{Hz} \tag{2}$$

Feedback resistance (R1 and R2) will contribute to the output noise by the inherent thermal noise of the resistors and through opamp noise current which ultimately must be considered.

The output current noise of the constant current loop is limited by the input voltage noise of U2 and U3. The magnitude of the noise contribution from U2 is inversely proportional to the resistance of $\mathrm{R_{sense}}$,

$$\mathrm{I_{noise}} = \frac{\mathrm{e_n}}{\mathrm{R_{sense}}} \tag{3}$$

where $\mathrm{e_n}$ is the input referred voltage noise of U2. The contribution of U3 to the current noise of the constant current loop is given by,

$$\mathrm{e_n} \frac{I_{\mathrm{max}}}{V-_{\mathrm{max}}} \tag{4}$$

where I_{max} is the maximum constant current, and $V-_{\mathrm{max}}$ is the voltage on the inverting input of U3 that corresponds to the maximum current. It is likely that Eq. 3 will be greater than Eq. 4 since $\mathrm{R_{sense}}$ is small.

Transient response

The response time of the CV loop is limited by the bandwidth of the pass transistor, Q1, in addition to the effects of unavoidable inductances associated with the wiring of Q1 and the output capacitance. As such, it appears that there is no advantage to using a very high speed opamp for U1. The phase delay of U1 is of great importance to the transient response, this will be discussed in detail later. U2 can be of relatively high speed such that the U2, Q3 and R4 combination form a tight local feedback loop with little phase delay with respect to the entire CC feedback loop.

Load regulation

Load regulation is limited by the DC loop gain. Since the loop gain is expected to be very large the load regulation is likely to be insignificant.

SPICE simulations

The schematic of the constant voltage analog section of the linear power supply as simulated using LTspice is shown in figure 2. The LT6233 opamp has been chosen for its very low noise, a gain-bandwidth product that is sufficient for a fast transient response and a phase delay that allows for good stability. To capture some of the realistic characteristics of the output capacitance a SPICE model of a 100 μF Rubycon aluminium polymer capacitor (50PZF100M10X9) was incorporated into the simulations. Inductances have also been included to represent pass transistor wiring.

Circuit description

The CV control loop is a negative feedback circuit and its dynamic behaviour can be understood in terms of the loop gain, A(s), and phase delay, ϕ(s), as a function of frequency. A necessary condition for stability is a loop gain of less than unity at the frequency where the phase delay is 360 degrees. An understanding of the behaviour of the CV loop is aided by small signal transfer function calculations of the transistor network shown in Fig. 3, the results of which are shown in Fig. 4.

Constant voltage loop

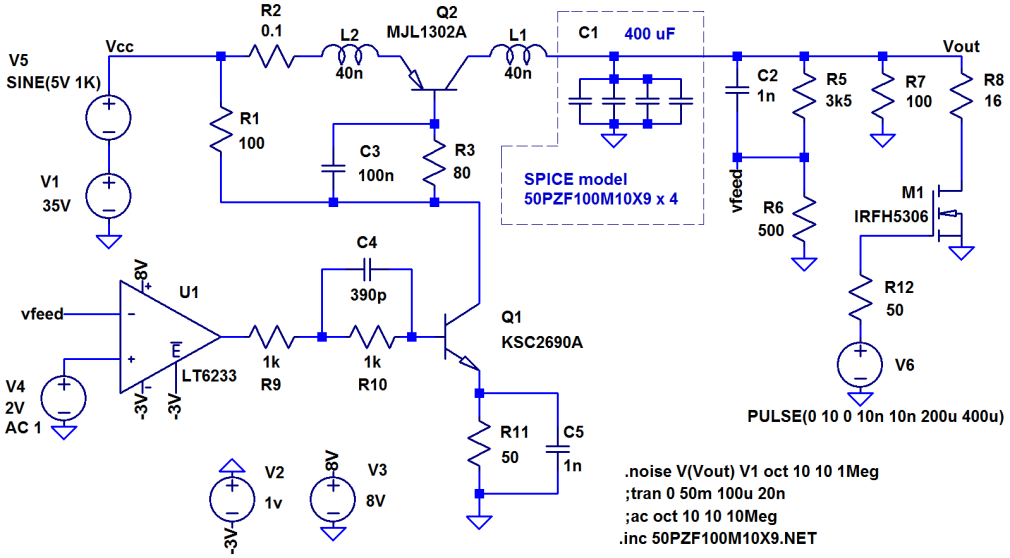

Figure 2: Schematic diagram of the constant voltage control loop as simulated by LTspice.

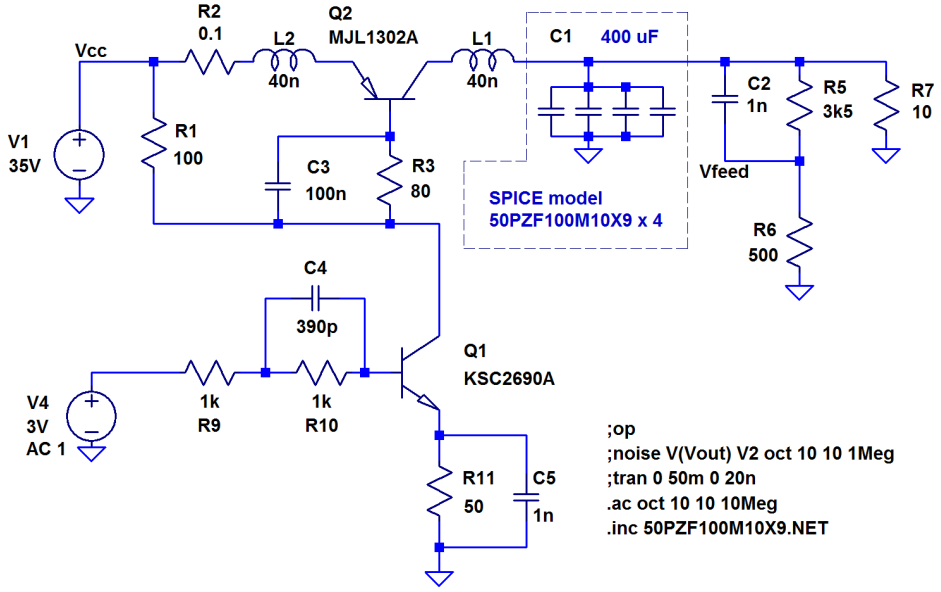

Figure 3: Schematic diagram of the transistor network as simulated by LTspice.

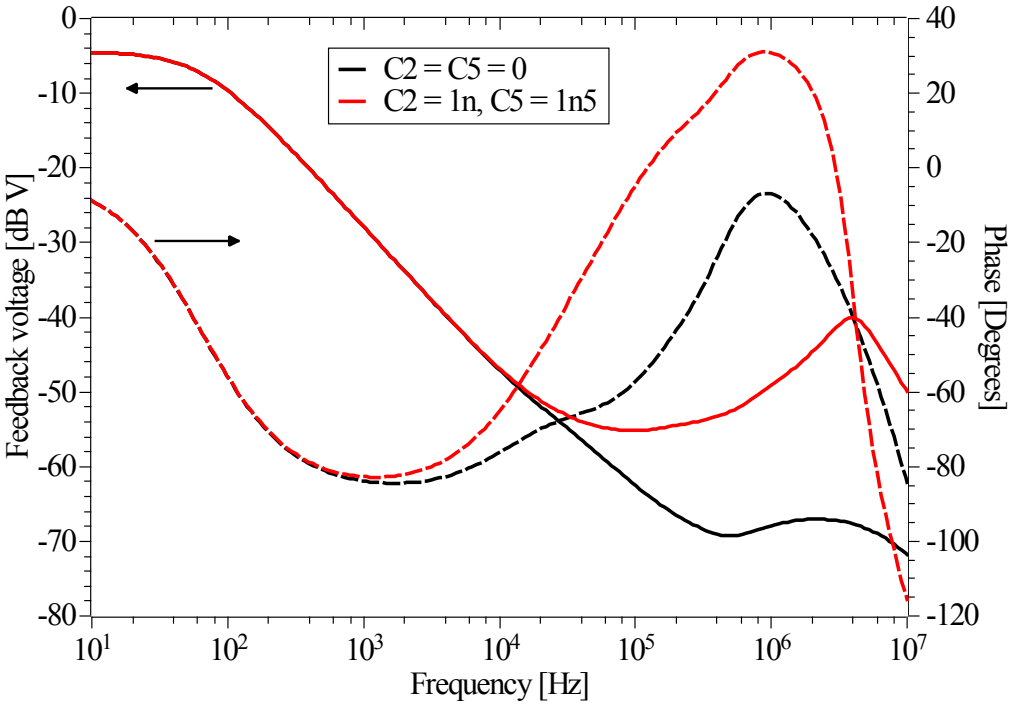

Figure 4: Small signal AC transfer function of the transistor network of the schematic shown in Fig. 3. V4 is the small signal input and Vfeed is the output.

At low frequencies the phase delay of the transistor network is minimal because the resistive load and output capacitance combination appears resistive. The phase then begins to decrease towards -90° as the output appears capacitive. At higher frequencies greater than 1 kHz the phase increases as the ESR and ESL of the output capacitors make the output appear resistive once again. For frequencies greater than about 1 MHz the phase decreases again due to the bandwidth limits of Q1 and Q2. C2 and C5 play the most critical role, they provides a phase lead around the 5 kHz to 50 kHz band, without which, the additional phase delay of the LT6233 opamp results in a marginal phase margin and ringing of the pass transistor in response to sudden changes in load current. The phase delay of the opamp at the lower frequencies where the phase delay of the transistor network approaches 90° clearly has a critical impact upon circuit stability. The LT6233 opamp has a phase delay sufficiently less than 90° within this critical frequency band. A higher-frequency oscillation may result if the loop gain does not decrease sufficiently for frequencies greater than a few MHz. Circuit simulations suggest that there are no high-frequency oscillations, however, if the actual circuit displays high-frequency instabilities then C5 can be removed since it has a strong impact upon loop gain at high-frequency, but only makes a small contribution to the low-frequency stability. Figure 6 is a plot of the calculated pass transistor collector current in response to a step change of the load current for the optimised component values as shown in Fig. 2 and for C2 = 100 pF. The importance of the phase lead created by C2 is evident.

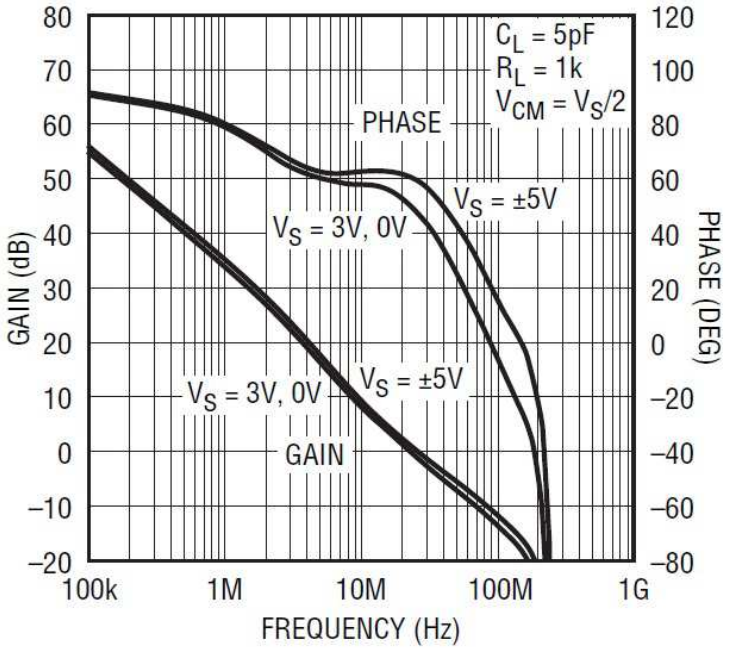

Figure 5: Open-loop gain and phase of the LT6233 opamp.

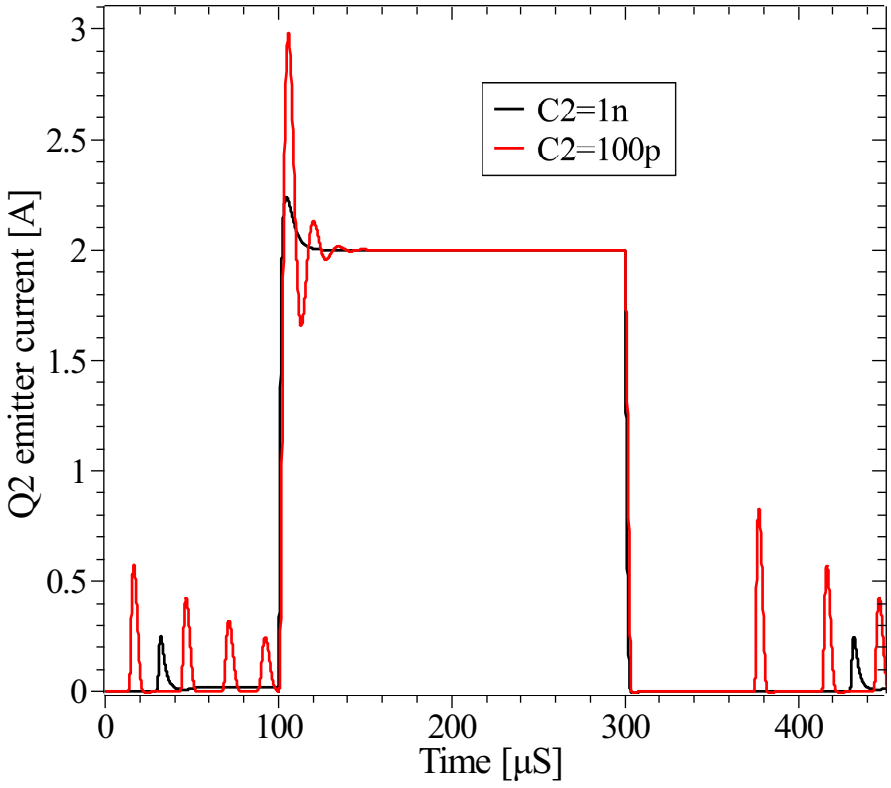

Figure 6: Simulated constant voltage loop response to a step increase of load current from 20 mA to 2 A.

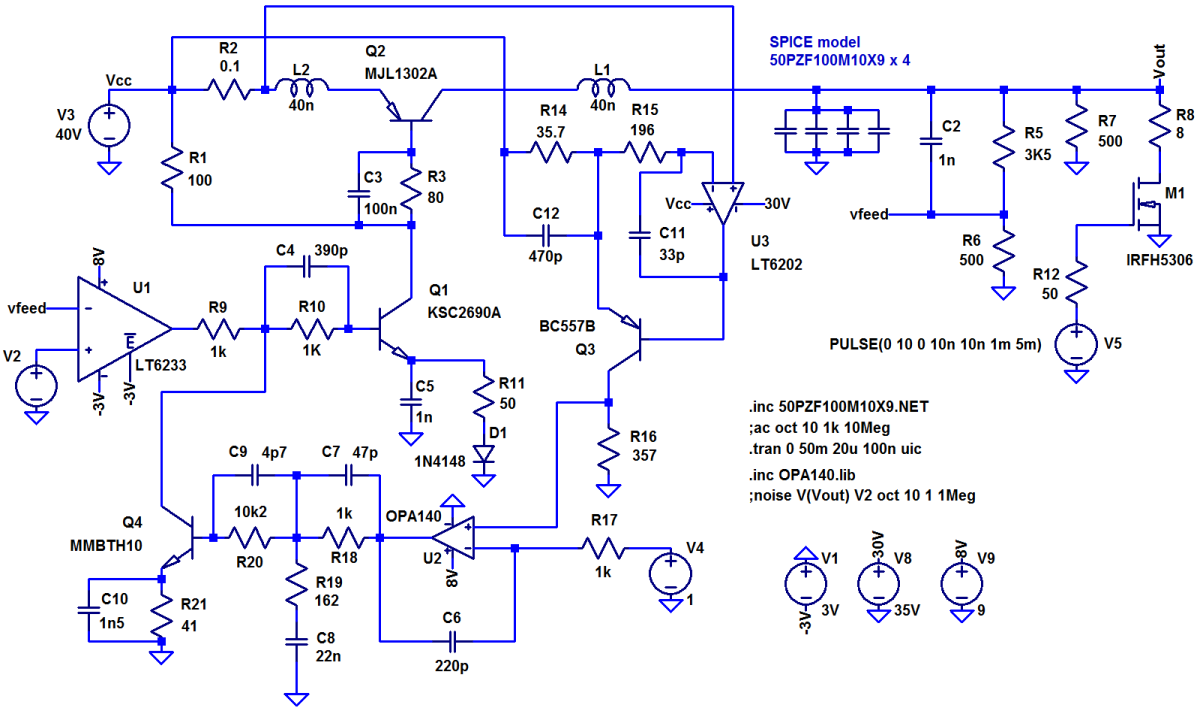

Figure 7: Schematic diagram of the CV and CC control loops as simulated by LTspice.

The full simulation schematic of the combined CV and CC control loops is shown in Fig. 7. Although the CC and CV loops shares circuitry the CC loop is compatible with optimal CV loop component values. The LT6202 opamp senses the voltage across R2 and together with R14, R16 and Q2 produces a voltage across R16 in proportion to the emitter current of Q2, $V_{\mathrm{R16}} = I_{\mathrm{E,Q2}}$. LT6202 has a relatively large gain-bandwidth product of about 100 MHz such that the voltage across R16 has little phase delay in response to the emitter current of Q2 at the frequencies of importance to the entire CC feedback loop. C12 produces a phase lead to assist in stability of the loop, while C11 ensures high-frequency stability of the LT6202 opamp. The OPA140 opamp compares the voltage across R16 to the current limit setting voltage. When V_{R16} becomes greater than the current limiting voltage the MMBTH10 transistor starts to conduct and draw current away from the base of Q1. C7, C9 and C10 provide a phase-lead. R18, R19 and C8 in addition to C6 reduces the loop gain at higher frequency. The net effect is a loop gain of less than unity at the frequencies where the phase delay is greater than 360°. The OPA140 opamp has an important property: There are no protection diodes connected between the inputs and large differential voltages are permissible without input current draw. This property is important since it permits a large current limit setting voltage to be present on the inverting input of U2 without interfering with the voltage across R16. Fig. 8 displays the response of the CC circuit to a step increase of load current with current limiting set to 0.5 A. The time taken to limit current is less than 10 μS with a settling time of about 50 μS. Fairly good...

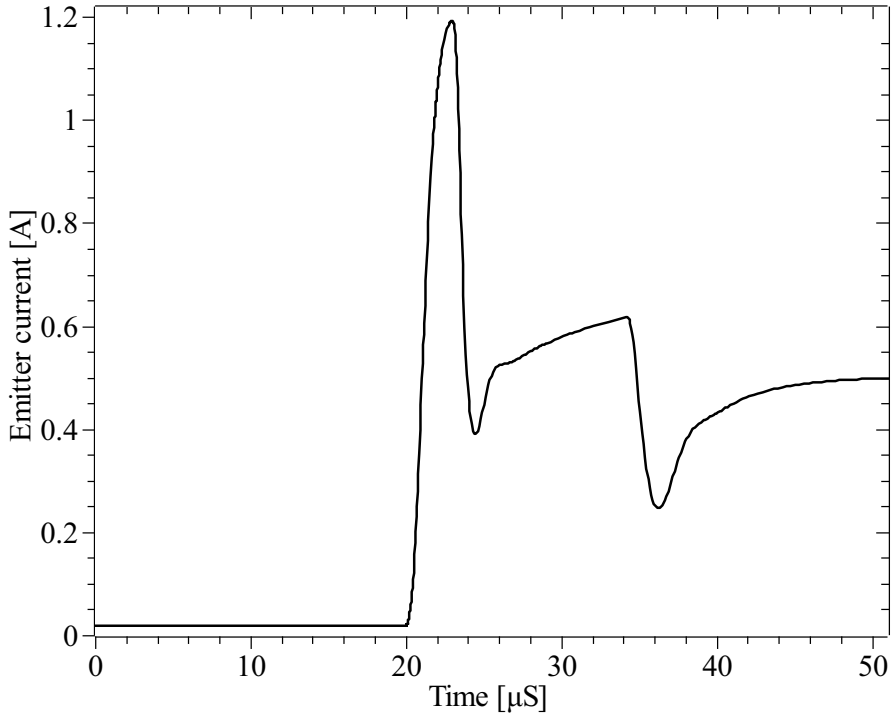

Figure 8: Simulated constant current loop response to a step increase of load current.

3 Analog prototype board

The analog sections of the power supply were prototyped and characterised. The prototype schematic diagram and PCB layout are shown in figures 10 - 12. The prototype schematic closely matches the SPICE simulation circuit, with the addition of opamp and reference voltage power circuitry. The prototype board was populated and characterised with the component values as shown in the schematic diagram. Careful consideration has (and must) be given to the PCB layout in order for the circuit to behave as intended. A substandard layout will degrade performance from optimal. The PCB layout can have an impact upon the following LPS characteristics in particular,

- Voltage regulation
- Ripple
- Excessive transient ringing / stability issues

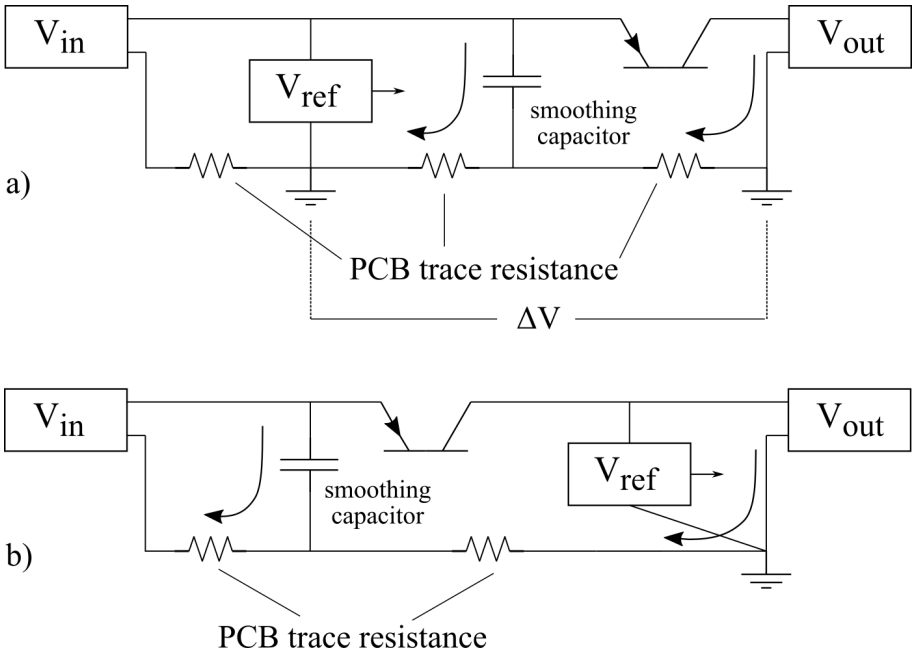

Figure 9: Diagram of a) poor PCB layout resulting in excess ripple due to current loops and b) the strategy used to minimise excess ripple.

Ground current loops can result in ripple and degraded voltage regulation as demonstrated in Fig. 9. Fortunately, the effects of ground current loops are easily minimised by following two strategies. All large currents, namely those associated with the input, filtering capacitors and the output load are isolated from the control loops. In addition, the point at which the control loops derive their ground potential is taken at output connector. Optimising the PCB layout in regards to transient response is a little bit more complicated. Consideration must be given to the effects of PCB parasitic capacitance, capacitive coupling and electromagnetic coupling. Parasitic capacitance can degrade phase margin and therefore stability and capacitive and magnetic coupling can result in unintentional feedback which can lead to stability issues.

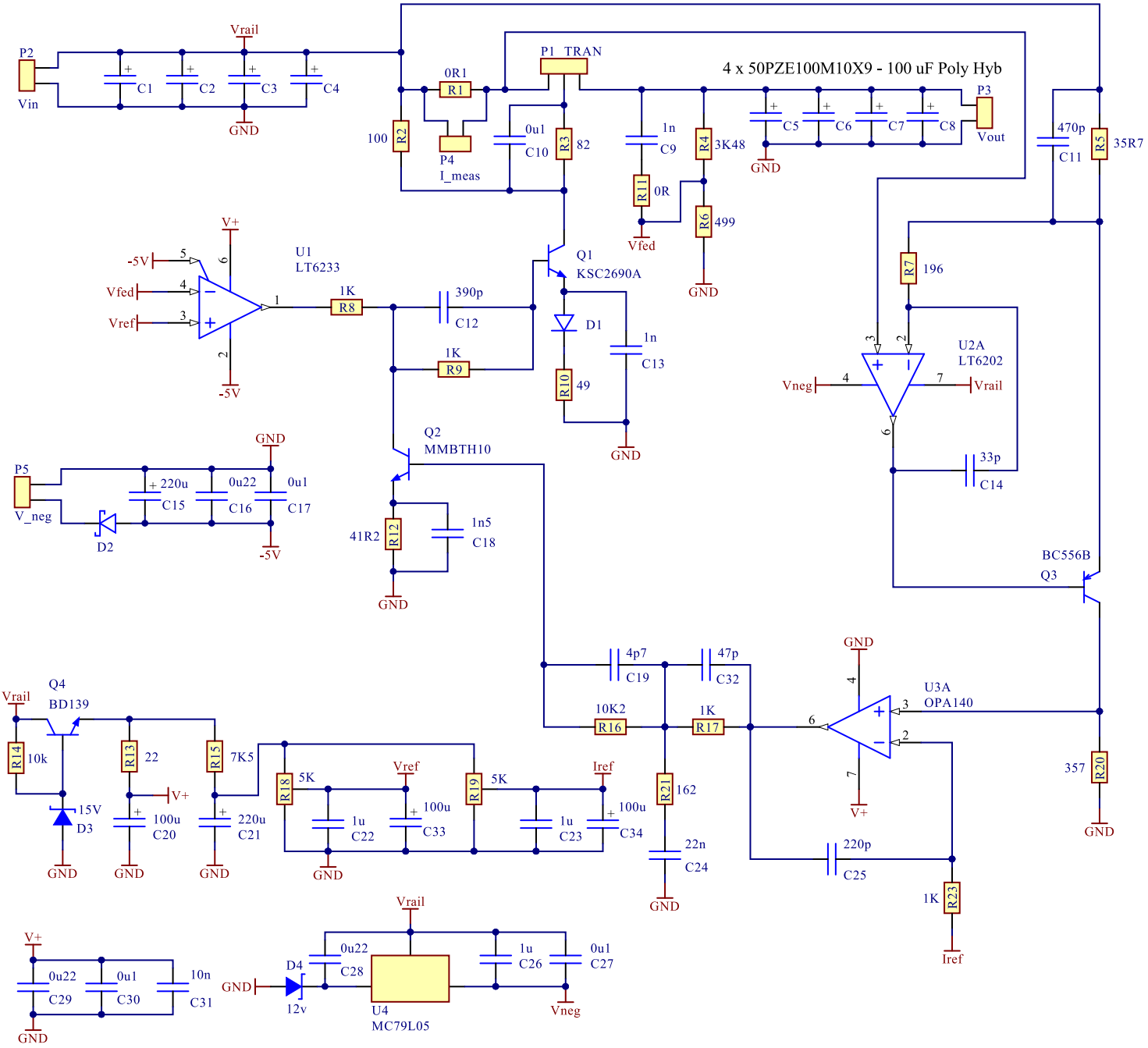

Figure 10: Schematic diagram of the analog prototype board.

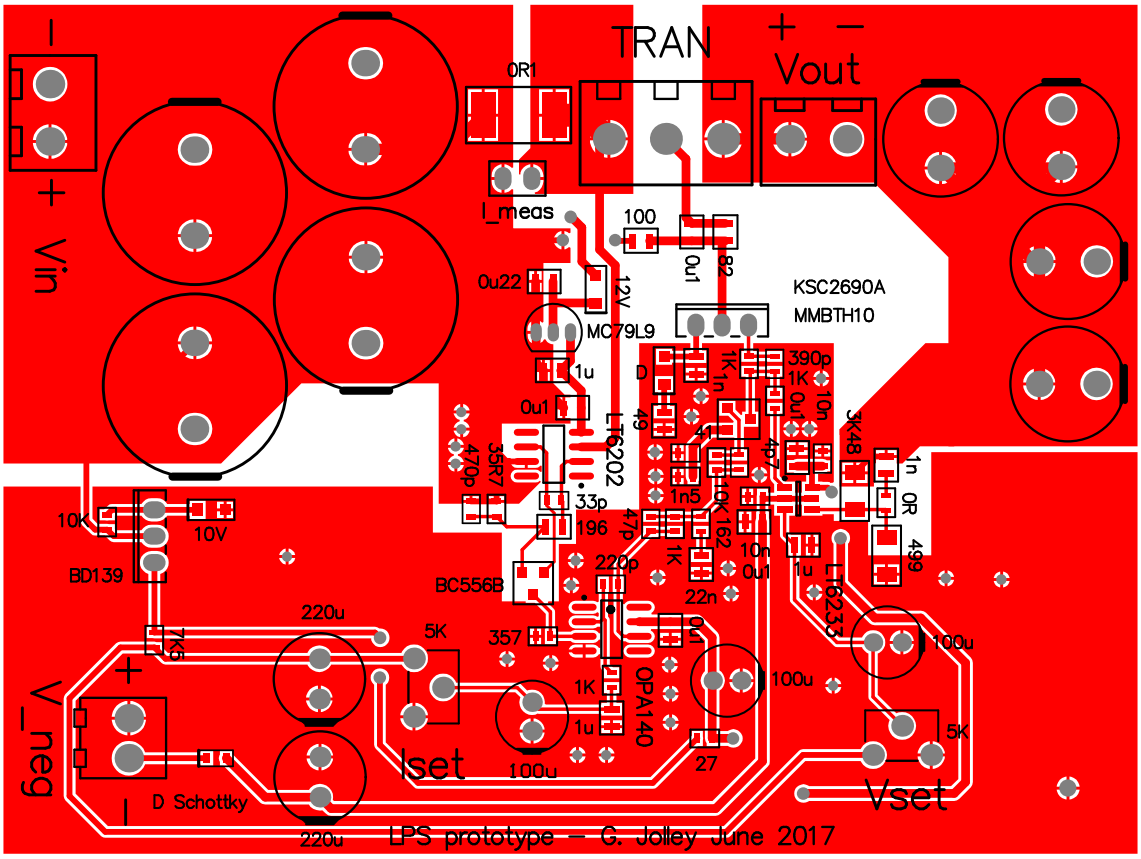

Figure 11: PCB top copper layer of the analog prototype board.

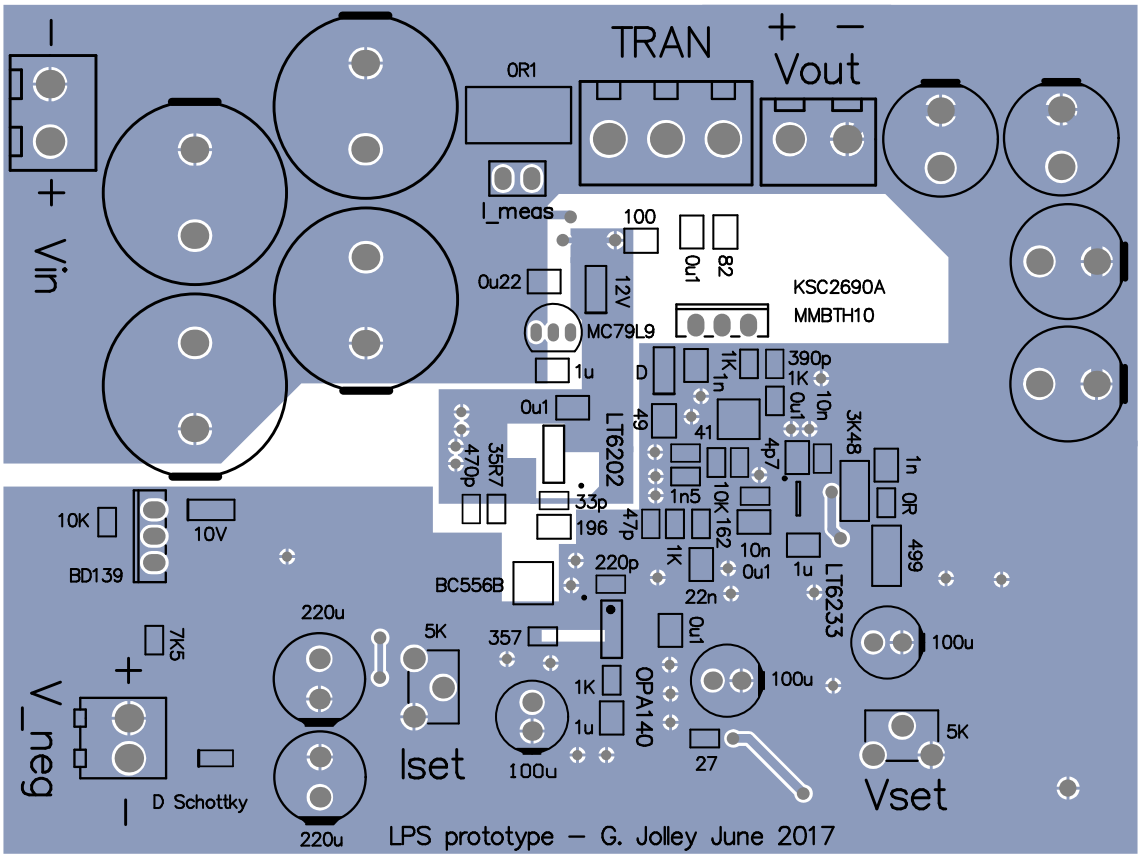

Figure 12: PCB bottom copper layer of the analog prototype board.

4 Prototype baord characterisation

Transient response

The transient response of the CV mode to a rapidly changing load current was captured by a circuit switching a 10 Ω load resistor by MOSFET with rise and fall times of the order of 20 nS with results shown in Fig. 13. The measured transient response is rather nice with a rise time of about 2 μS, an overshoot of 15% and no ringing. These value compare very well with simulation. In a similar manner the response of the CC loop was obtained. The current limit was set to 0.5 A and a resistive load was switched on and off, results shown in figure 14. Initially, in response to the sudden load increase, the pass transistor current overshoots to 0.74 A due a the time delay associated with the CC mode circuit. The response of the CC loop is rapid with a current overshoot lasting only 6 μS.

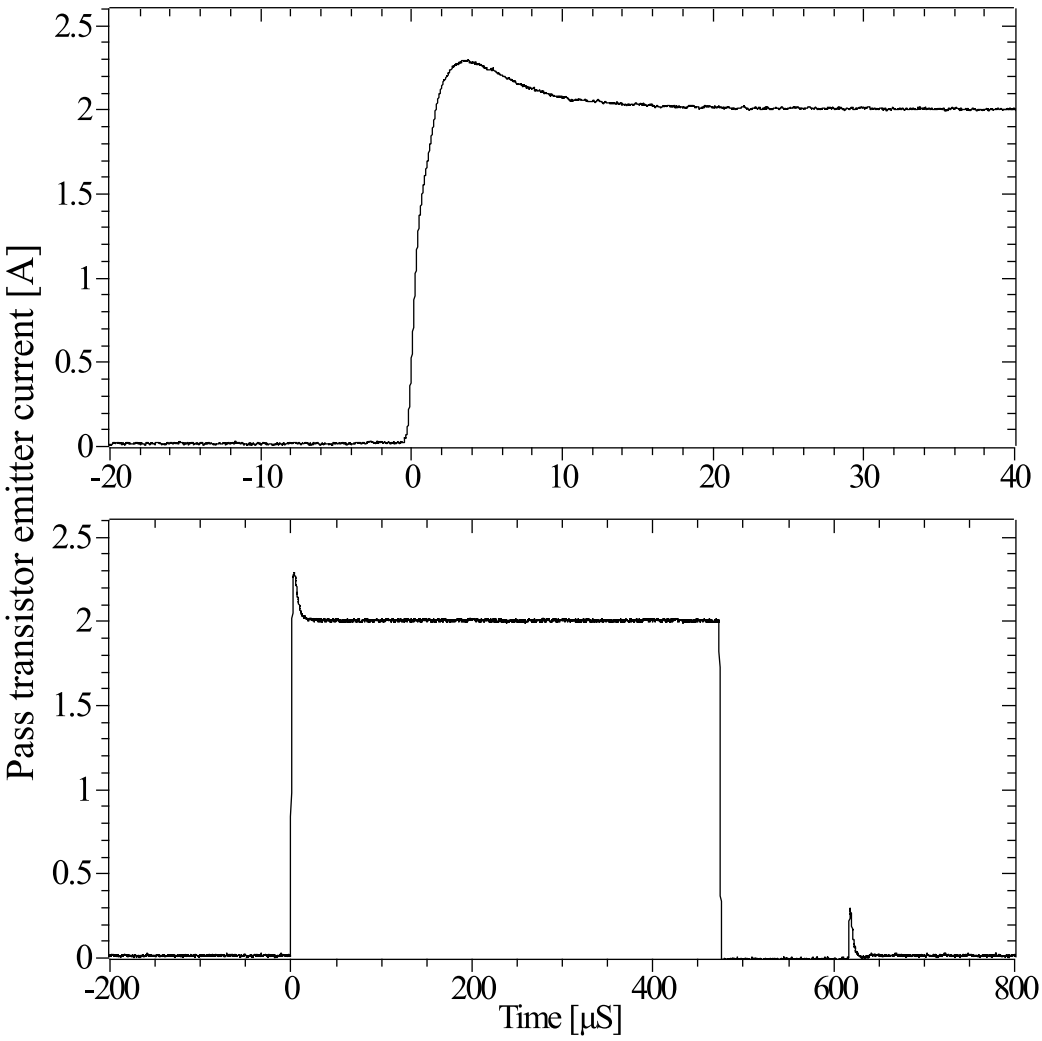

Figure 13: Measured constant voltage loop response to a step increase of load current from 20 mA to 2 A.

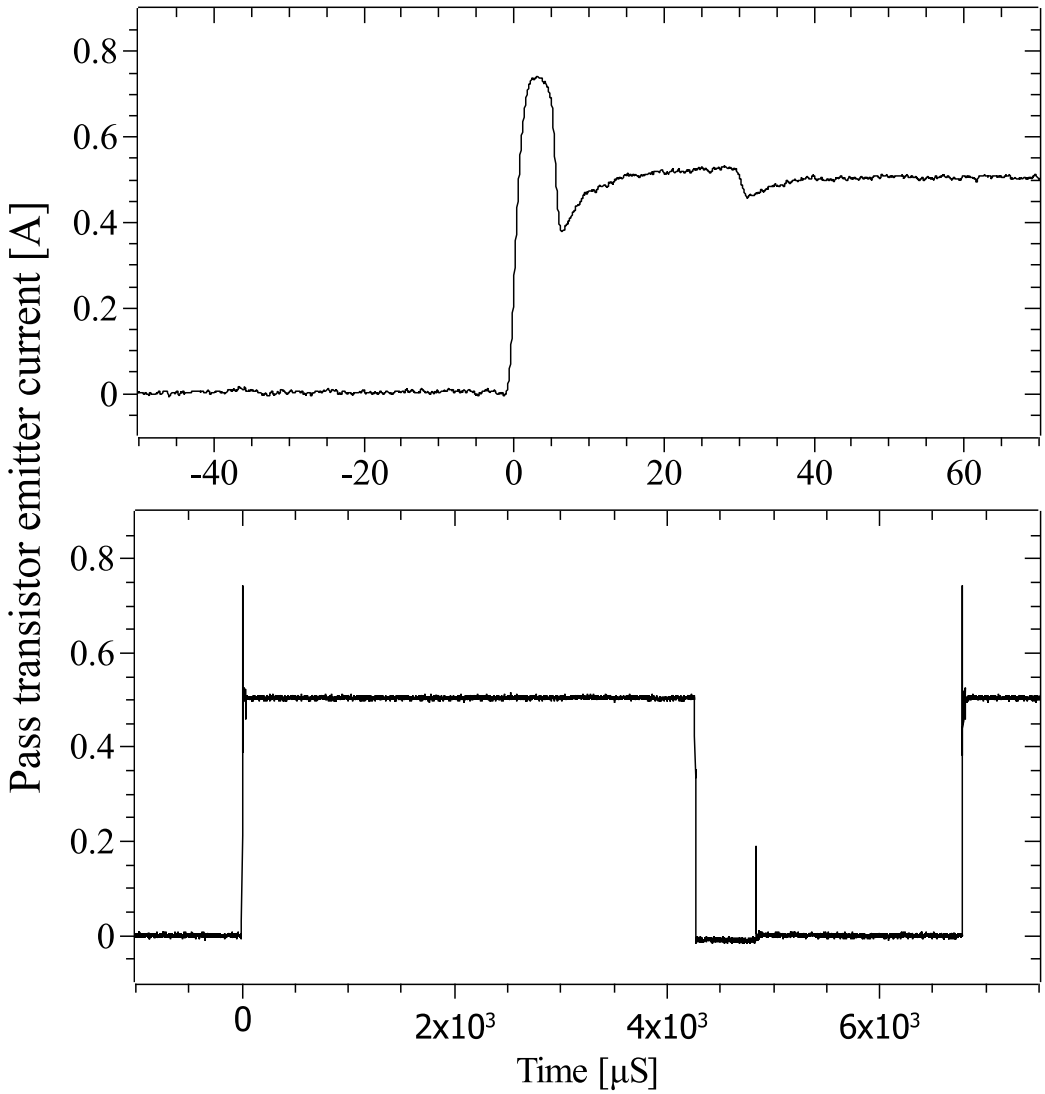

Figure 14: Measured constant current loop response to a step increase of load current.

Noise

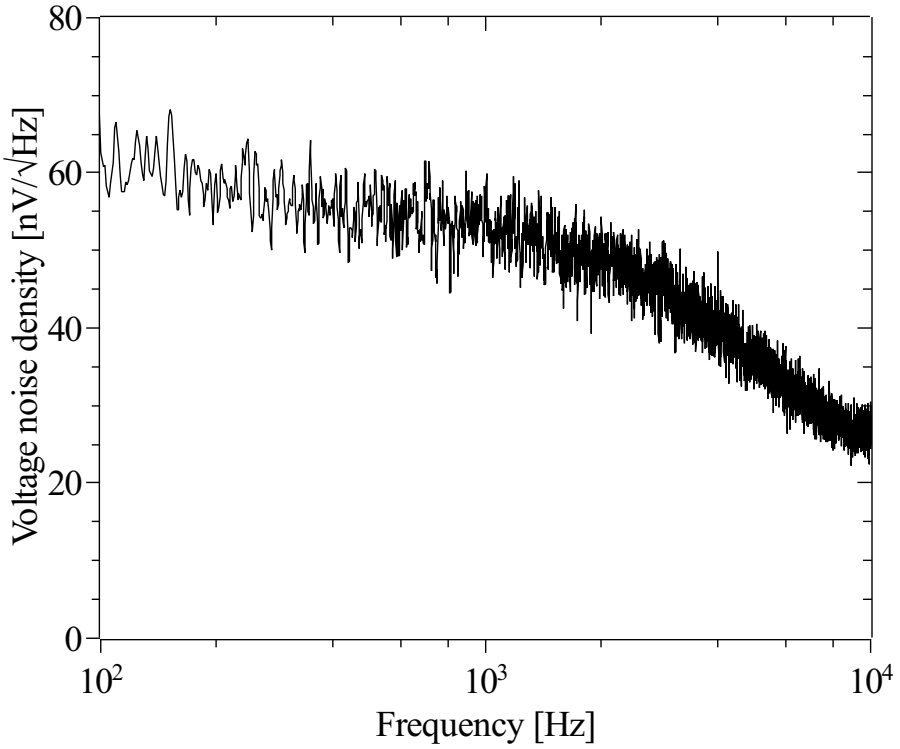

Figure 15: Output voltage noise spectrum.

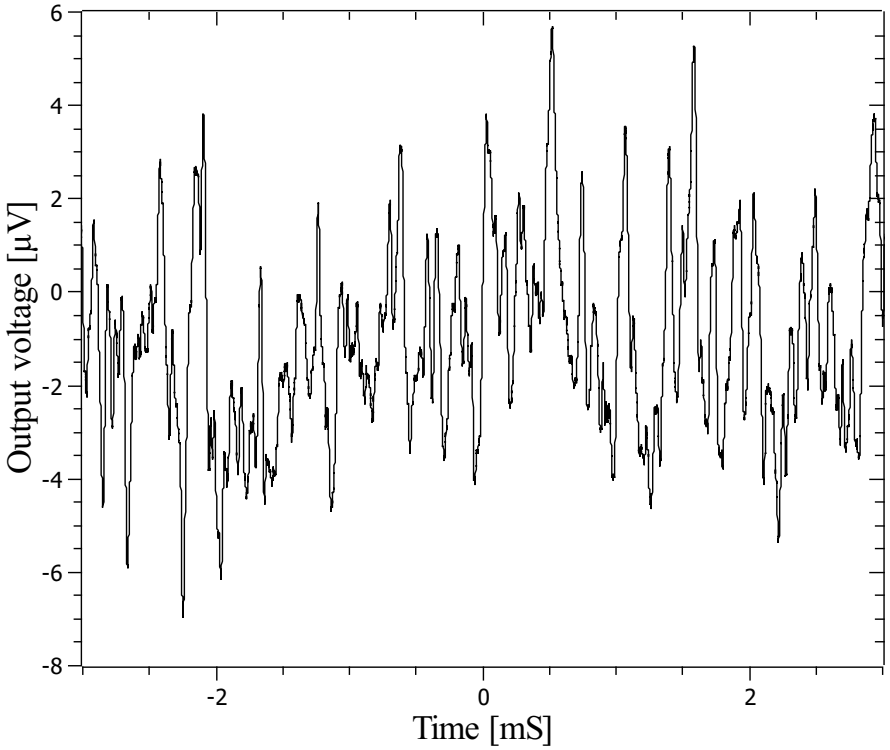

Figure 16: Output voltage noise within the 10-10 kHz band.

Those sources which significantly contribute to the output voltage noise are well known and the magnitude of the noise is easily calculated. In CV mode the noise sources are:

- The voltage and current input referred noise of opamp U1
- The thermal noise of feedback resistors R4 and R6 and potentiometer R18

Sources of noise within the feedback loop have minimal impact upon the output noise since the negative feedback loop minimises their influence. The output voltage noise density at frequencies greater than about 1 kHz, such that R18 has little effect and the LT6233 is within its flat band noise region is calculated to be,

$$\frac{R4+R6}{R6}\left[\mathrm{e_n^2}+\mathrm{I_n^2}\left(\frac{R_4R_6}{R_4+R_6}\right)^2+4k_BT\frac{R_4R_6}{R_4+R_6}\right]^{1/2} \tag{5}$$

$$8\left[\left(1.9\times10^{-9}\right)^2+\left(7.8\times10^{-13}\times438\right)^2+438\times4\times1.38\times10^{-23}\times300\right]^{1/2}\ \mathrm{V}/\sqrt{\mathrm{Hz}} \tag{6}$$

$$=26.5\,\mathrm{nV}/\sqrt{\mathrm{Hz}} \tag{7}$$

This value is very must less than the upper specification limit of 158 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$. The voltage and current noise of the LT6233 opamp increases for frequencies less than 1 kHz and 100 Hz respectively.

Spectrum analysis result

The power supply noise within the 20 - 10 kHz band was measured by connecting the output up to a low-noise amplifier with a gain of 80 dB. Output noise of the CV mode was captured in the frequency and time-domain, the results of which are shown in figures 15 and 16. This result can be compared with the LTspice result shown in figure 17. There is very agreement between the calculated, and simulated noise values. However, the measured noise spectrum is somewhat larger than expected for frequencies less than about 5 kHz.

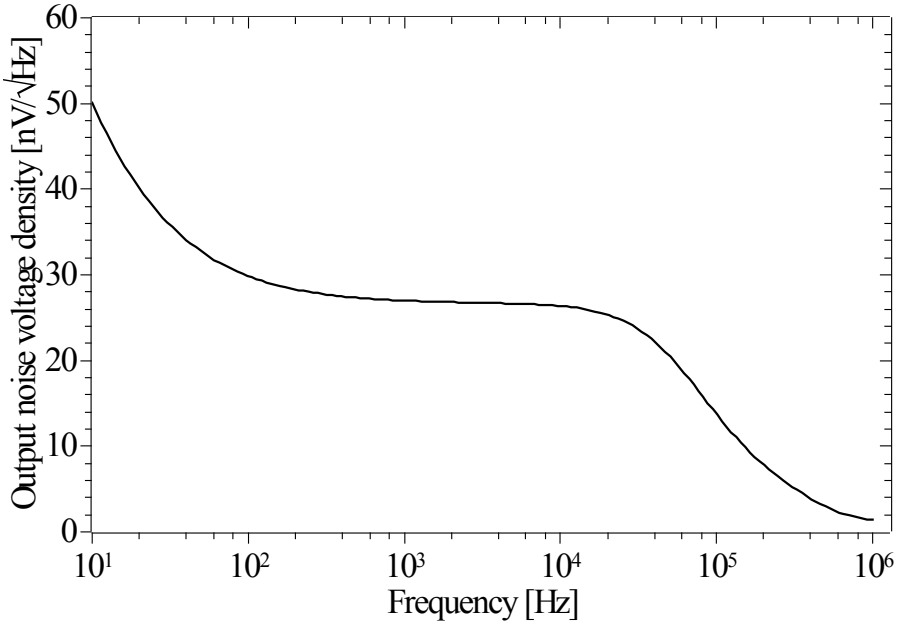

Figure 17: Simulated output voltage noise spectrum of the CV loop.