Benchtop linear power supply: design, construction and characterisation

G. Jolley

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Abstract

This document describes the design, simulation, construction and characterisation of a versatile 3-channel general-purpose benchtop linear power supply. Features include current limiting and digital control of the supply parameters. The two main channels have a voltage range of 0-32 V and a constant current range of 0-4 A. The third, lower voltage channel has a voltage and constant current range of 0-8 V and 0-4 A. All channels are electrically isolated and exhibit very low-noise and ripple of less than 50 μV_{RMS}. Both the constant voltage and constant current modes have a transient response time of less than 10 μS. This is work in progress, results are added as they are obtained.

Contents

1 LPS features, characteristics and design goals

Power supply features

Although a power supply can be considered as performing a single function; provide an appropriate and constant voltage to a load irrespective of any time dependent current requirements, additional features greatly increase its versatility. A general-purpose benchtop power supply must have two supplies at a minimum to allow for the powering of split-rail analog circuits. The addition of a third, lower voltage supply is useful for powering mixed analog and digital circuits. Current limiting is indispensable for R&D purposes to minimise circuit destruction under fault conditions. A constant current mode has many applications beyond circuit protection and some circuits are naturally powered by a constant current. Digitally controlling and monitoring the power supply voltage, load current and current limit enhances functionality. For example, microcontroller routines can be written for battery charging applications or circuit and component I-V characterisation.

The upper supply voltage and current capability must be chosen. Increasing the voltage and current capability extend the usability of the supply, all-be-it with diminishing returns. An increase of the voltage capability comes with increasing thermal dissipation management and transformer size costs. An upper voltage of about 35 V and a continuous current capability of 4 A are tentatively chosen. A list of the chosen power supply features include:

- Two independent and electrically isolated voltage adjustable channels with a 35 V and 4 A capability.
- A third adjustable lower-voltage channel intended for the powering of digital circuits, also electrically isolated.
- Analog constant current and digital shutdown protection modes on all channels.
- Digital control of the voltage and current limit, 1 mV and 1 mA resolution.
- Load current and voltage readout, 1 mV and 1 mA resolution.
- Computer USB interface for data logging.

A conspicuously absent feature is remote sensing which is used to tightly regulate the supply's output voltage at the load. Although remote sensing is unlikely to be significantly difficult to implement I have decided to leave this feature out, perhaps for a future version. A single user interface board shall communicate with the 3 power boards and handle all user interface and data logging tasks. A description of the third, lower voltage supply and the user interface is given after a complete description the main supplies.

Brief statements on LPS characteristics

All power supplies exhibit nonideal behaviour. The following three parameters are commonly used to specify power supply quality,

- Noise and ripple
- Load regulation
- Transient response

Noise

Power supply noise may adversely influence the performance characteristics of some circuit classes and must be explicitly considered. Note, voltage and current noise are considered for constant voltage and constant current modes of operation respectively. Two types of noise are present on the output of a power supply; wideband and ripple. Wideband noise is the result of fundamental physical mechanisms such as resistor thermal noise and can be minimised, but not eliminated. A number of mechanisms may contribute to output ripple including a poor PCB layout. Certainly, voltage ripple will occur due to a combination of input ripple along with the pass transistor early voltage and the finite loop gain at the ripple frequency. Integrated over the frequency band 10 Hz-100 kHz, a total output noise voltage of 50 μV_{RMS} is an excellent noise figure for a linear power supply while reasonable easy to achieve (I think...) and is chosen as the maximum specification limit. Circuits utilising a constant current usually have a greater tolerance to noise. At this stage I do not have a concrete idea of what current noise figure will be reasonably achievable.

Load regulation

Load voltage regulation indicates the degree of dependence that the output voltage has on the static load current and is defined by the equation,

$$\% \text{ Voltage regulation} = 100\% \frac{\Delta V_{\text{out}}}{V_{\text{out}}} \frac{I_{max}}{\Delta I_{\text{load}}} \tag{1}$$

Similar for current load regulation,

$$\% \text{ Current regulation} = 100\% \frac{\Delta I_{\text{out}}}{I_{\text{out}}} \frac{V_{max}}{\Delta V_{\text{load}}} \tag{2}$$

Voltage regulation is dependence on the DC loop gain and is likely to be insignificant.

Transient response

Sudden changes in load current result in transient fluctuations of the supply voltage. When designing a power supply great attention must be given to its transient behaviour since it indicates the degree of stability of the power supply, which must be ensured for all possible load conditions. In addition, excessive ringing of the output voltage in response to sudden changes of load current can be considered as load induced noise. Given the characteristics of a good, general purpose power transistor, it is reasonable to aim for a settling time of less than 10 μS of the pass transistor current to a step increase of load current.

Current limit response time

The response time of the current limit should be sufficiently short to minimise circuit destruction. However, capacitance at the supply output will limit the effectiveness of a fast response due to the stored charge. Placing a fast crowbar across the supply output can counter the effect of stored charge.

Voltage and current readback resolution and accuracy

Digital-to-analog converters are an ideal choice for setting the output voltage and current limit. In addition, analog-to-digital converters will be used to read the output voltage (a necessary requirement if the voltage is limited by current protection) and load current. It is expected that the values read by the ADCs will be used as feedback to made small correction to the output voltage and current limit, therefore, the output accuracy will be limited by the accuracy of the readback circuitry.

Typically a circuit does not require a precision set supply voltage and a voltage setting resolution of ± 0.1 V is adequate for a large number of applications. There are numerous exceptions including component I-V characterisation and battery charging. For example, diode characterisation is best performed at a voltage resolution that is less than the thermal voltage, $V_{th} = k_{\text{B}}\text{T/e} = 26$ mV at room temperature. The voltage and current limit setting resolutions shall be 1 mV and 1 mA. The voltage and load current readback will have a similar resolutions. Assuming the voltage readback is calibrated for offset and gain, perhaps by trimpot adjustment, factors influencing the accuracy can be categorised as either drift or temperature dependent. A precision voltage readback accuracy can be achieved by a brute force and expensive method, namely, utilize precision voltage reference ICs, accurate and high resolution ADCs and use voltage divider resistors with a very low temperature coefficient of resistance. A better engineered solution may be to utilise any information about the temperature dependence of components and provide a temperature correction. Drift is usually a much harder variable to predict and therefore correct. Fortunately drift often occurs over extended periods of time and can be corrected by performing routine calibrations. Accuracies of 0.1% and 1% are chosen as the design goals for voltage and load current readback respectively, for operation within an ambient temperature range of 20-35°C. A voltage accuracy of 0.1% is sufficient for the vast number of applications and not too costly to achieve. Given the power supply analog topology to be shown next, a load current accuracy of less than 1% is not overly realistic. An offset error is also expected such that the load current and voltage error will be off the form,

$$\begin{aligned} \text{V}_{\text{error}} &= \text{V} \times 10^{-3} + \text{V}_{\text{offset}} \\ \text{I}_{\text{load}} &= \text{I}_{\text{load}} \times 10^{-2} + \text{I}_{\text{offset}} \end{aligned} \tag{3}$$

Offset errors can be corrected to a large degree by a static offset correction, although some temperature and drift dependence is expected. Critical to some applications is differential error. Consider monitoring small changes in the load current of a circuit over time and temperature. A gain error of 1% is unlikely to be of much consequence. The differential error has a much greater impact of measurement results over small variations.

2 Power board analog design

2.1 Topology

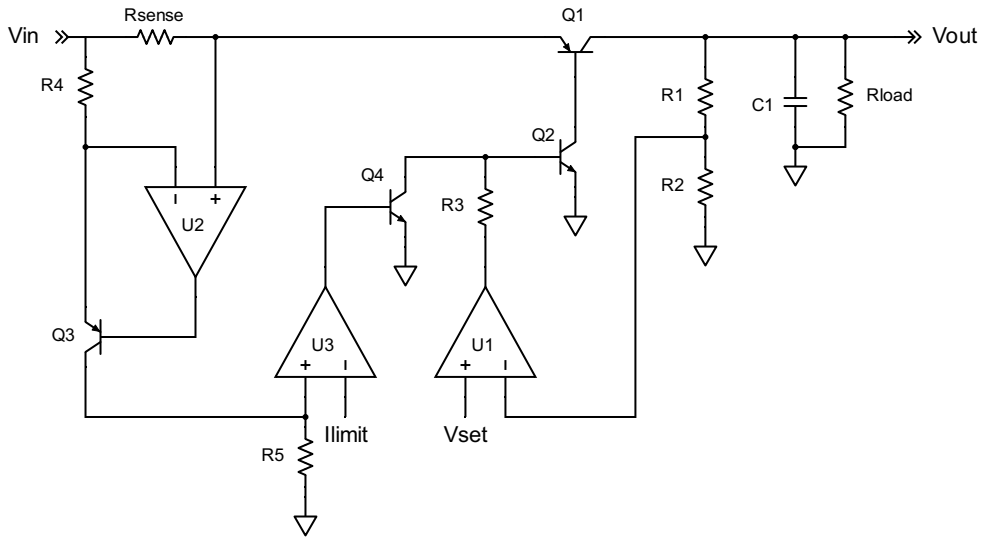

Figure 1: Simplified topology of the constant voltage and constant current control loops.

The simplified proposed topology of the constant voltage (CV) and constant current (CC) control loops is shown in figure 1. Opamps are an ideal choice for central use in the control loops since low cost and high performance options are available.

Opamp requirements

Given the topology some approximate opamp specification requirements can be determined to assist in the selection process before performing simulations.

Noise

The wideband output voltage noise of the CV loop is ultimately limited by the input noise of the opamp, U1 (of figure 1). Reference voltage noise and thermal noise of the feedback resistors (R1 and R2) also contribute to the voltage noise. Reference voltage noise can be filtered, although, filtering low-frequency noise might be cumbersome. Within the frequency band 10 Hz-100 kHz a total output noise voltage of 50 μV_{RMS} is a low noise figure for a linear power supply and is chosen as the maximum specification limit. If noise is dominated by the opamp voltage noise its density, $\mathrm{e_n}$, must be less than,

$$\mathrm{e_n(U1)} < \frac{50\,\mu\mathrm{V}}{\sqrt{10^5 - 10}} \frac{\mathrm{R2}}{\mathrm{R1{+}R2}} = \frac{\mathrm{R2}}{\mathrm{R1{+}R2}} \times 158\,\mathrm{nV_{RMS}}/\sqrt{\mathrm{Hz}} \tag{4}$$

Feedback resistance (R1 and R2) will contribute to the output noise by their inherent thermal noise and through opamp noise current which ultimately must be considered. At any rate, the magnitude of voltage ripple is yet to be addressed and it might have a tendency to dominate the total noise magnitude.

The output current noise of the constant current loop is limited by the input voltage noise of U2 and U3. The magnitude of the noise contribution from U2 is inversely proportional to the resistance of $\mathrm{R_{sense}}$,

$$\mathrm{I_{noise}} = \frac{\mathrm{e_n(U2)}}{\mathrm{R_{sense}}} \tag{5}$$

The contribution of U3 to the current noise of the constant current loop is given by,

$$\mathrm{e_n(U3)} \frac{\mathrm{I_{max}}}{\mathrm{V{-}_{max}}} \tag{6}$$

where I_{max} is the maximum constant current, and $V-_{max}$ is the voltage on the inverting input of U3 that corresponds to the maximum current. It is likely that Eq. 5 will be greater than Eq. 6 since R_{sense} must be significantly smaller than 1Ω.

OPAMP bandwidth/transient response

The transient behaviour (and associated stability) of the CV loop in response to sudden changes of load current is determined by the loop gain and phase as a function of frequency. A necessary condition for stability is a loop gain of less than unity at frequencies where the phase delay is 360 degrees. The combined phase delay of U1, Q1 and Q2 would result in high-frequency instability if not for the output capacitance (C1) which decreases the loop gain with increasing frequency. The equivalent series resistance of C1 also has a critical impact upon circuit stability, at higher frequencies ESR makes C1 appear resistive and therefore improves the phase margin. However, if the ESR is too large the loop gain will be greater than unity at frequencies where the phase delay is 360°. At moderate frequencies the output capacitance and load resistance combination contribute a 90° delay to the phase. Considering the above, the phase delay of a slow opamp combined with the phase delay of the output capacitance is likely to result in marginal stability at moderate frequencies. Likewise, a very fast opamp can result in high frequency instability if its gain is excess at frequencies where the phase delay of Q1, Q2 and U1 sum to 180°. Therefore, a moderate gain-bandwidth product is likely to be suitable for U1. At any rate, the response time of the CV loop is limited by the speed of the pass transistor so there is little value of a very high speed opamp.

On the other hand, U2 of the CC loop can be of relatively high speed such that the U2, Q3 and R4 combination form a tight local feedback loop with little phase delay with respect to the entire CC feedback loop. Ideally U2 has an input common mode range that includes its positive supply voltage, otherwise an additional supply voltage greater than Vin is required. The CC loop does not have a mechanism to reduce loop gain with frequency that is equivalent to the effect of C1 on the CV loop. Therefore, Opamp, U3, requires the smallest bandwidth and it is likely that an additional mechanisms to reduce gain at higher frequencies will be required.

2.2 SPICE simulations

The constant voltage circuit as simulated by LTspice is shown in the schematic of figure 2. Many simulations were performed, first to assist in the understanding of the circuit dynamics, and then to optimise the component values, of which are indicated in the schematic. Ultimately the LT6233 opamp was chosen due to its very low voltage noise, a gain-bandwidth product that is sufficient for a fast transient response and a phase delay that allows for good stability. Since the output capacitance magnitude and ESR influence the circuit dynamics its advisable to perform simulations with those characteristics of the intended capacitors of the final product. Aluminium polymer capacitors are found to assist in stability at higher frequencies due to their very low ESR. To capture some of the realistic characteristics of the output capacitance a SPICE model of a 100 μF Rubycon aluminium polymer capacitor (50PZF100M10X9) was incorporated into the simulations. Inductances have also been included to represent pass transistor wiring.

Circuit description

The CV control loop is a negative feedback circuit and its dynamic behaviour can be understood in terms of the loop gain, A(s), and phase delay, ϕ(s), as a function of frequency. An understanding of the behaviour of the CV loop is aided by small signal transfer function calculations of the transistor network shown in Fig. 3, the results of which are shown in Fig. 4.

Constant voltage loop

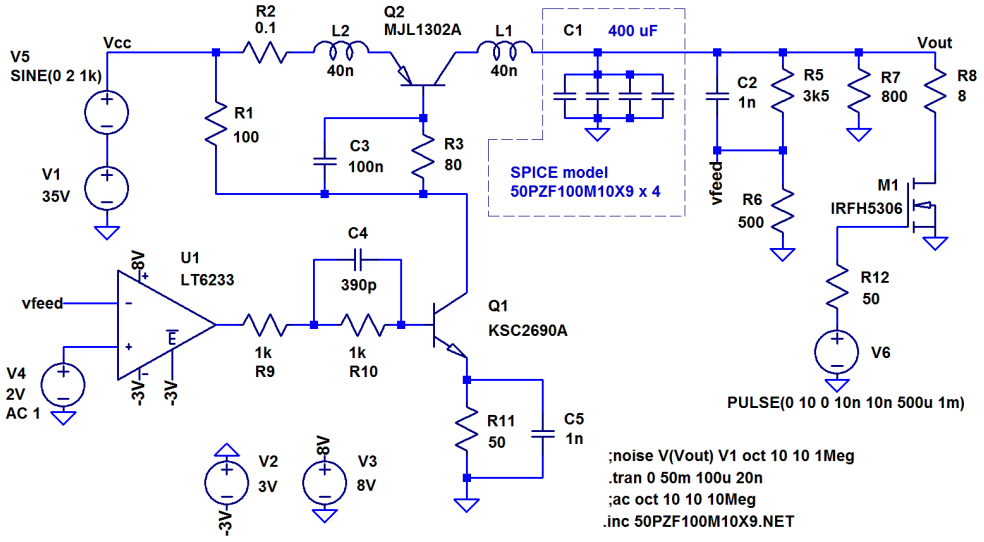

Figure 2: Schematic diagram of the constant voltage control loop as simulated by LTspice.

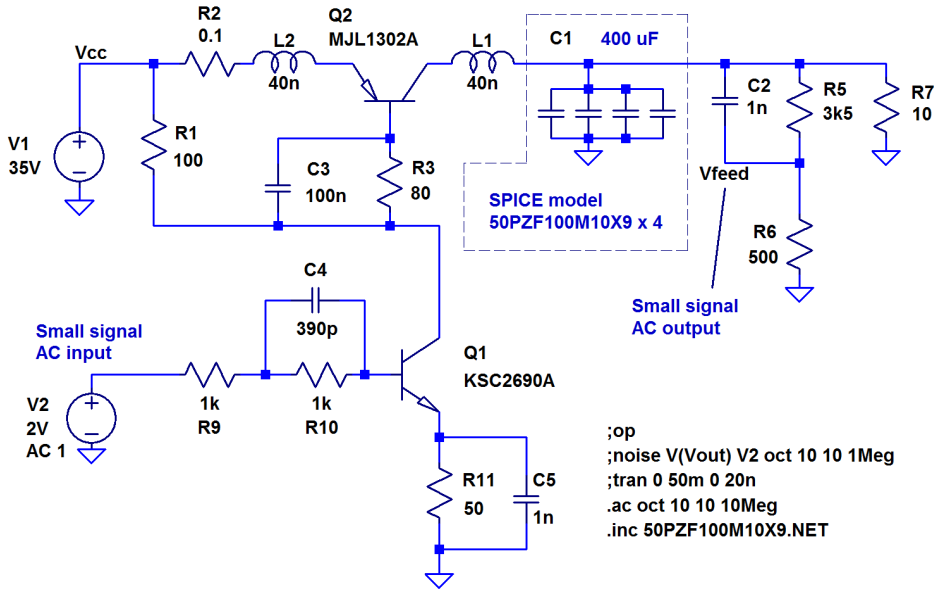

Figure 3: Schematic diagram of the transistor network as simulated by LTspice for small signal AC response.

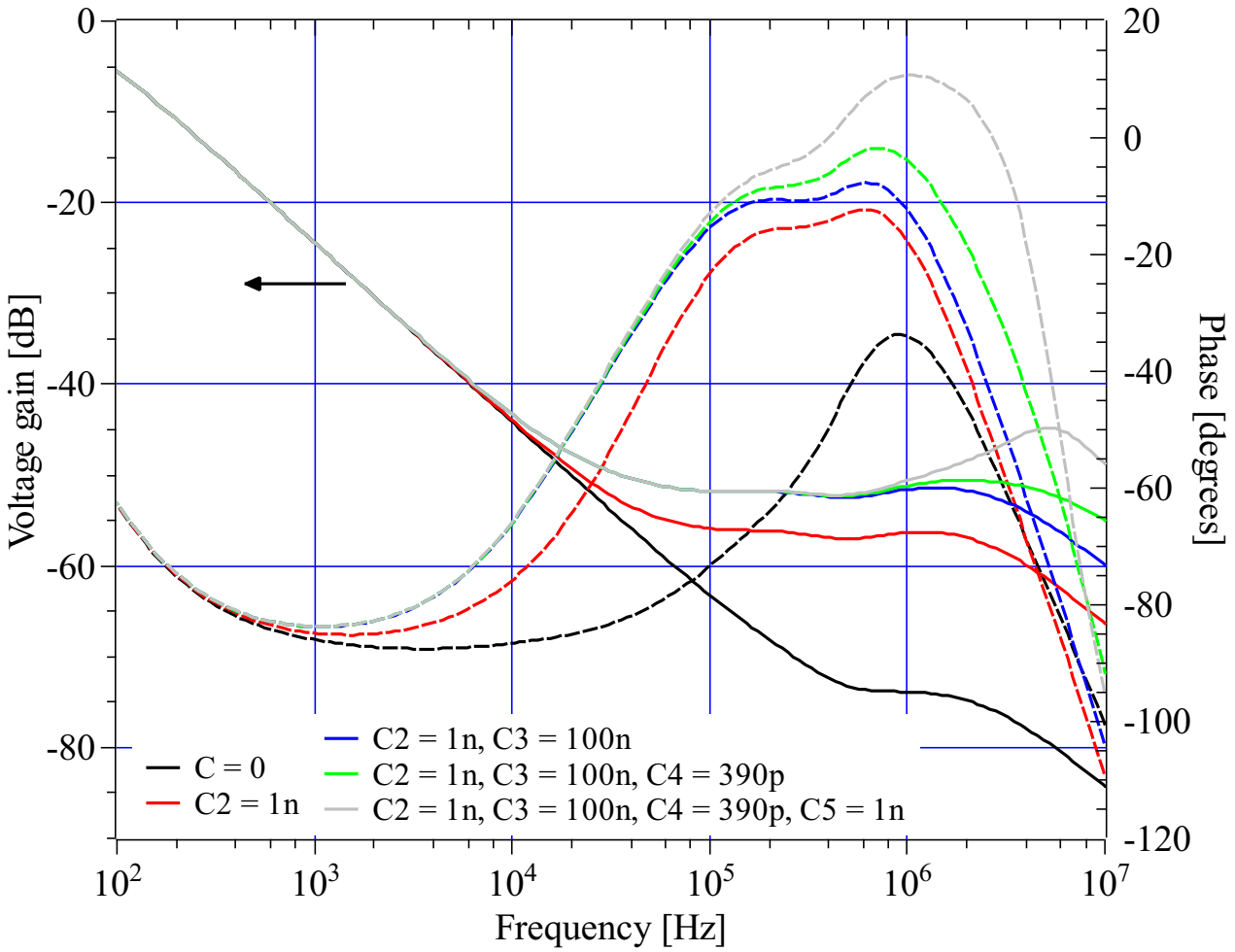

Figure 4: Small signal AC transfer function of the transistor network of the schematic shown in Fig. 3. V2 is the small signal input and Vfeed is the output.

The influence of the various capacitors on the phase and gain of the transistor network is gleamed by the numerous plots, starting with the presence of only output capacitance (C1), an additional capacitor is included with each plot. At very low frequencies the phase delay of the transistor network is minimal because the resistive load, R7, and output capacitance, C1, combination appears resistive. The phase then begins to rapidly decrease towards -90° (load resistance dependent) as the output appears capacitive. At frequencies greater than a few kHz the phase increases due to a number of contributions. For frequencies greater than about 1 MHz the phase decreases again due to the bandwidth limits of Q1 and Q2. At frequencies greater than 10 kHz the phase increases as the ESR and ESL of the output capacitors make the output appear somewhat resistive once again. The phase delay and associated effects of the capacitors requires careful attention within the the critical 1 kHz-100 kHz band. The 1 kHz-100 kHz frequency band is hereafter referred to the low-frequency critical band. The additional phase delay of the LT6233 opamp which is present for the entire CV loop pushes the total phase delay towards 360° within the low-frequency critical band. Note, the loop gain including the LT6233 opamp is much greater than unity at these frequencies. C2 induces a significant reduction of the phase delay within the critical low-frequency band. C2 increases the loop gain by a factor of 8 at higher frequencies which has the potential to impact stability within this frequency region. C3 also significantly reduces the phase delay within the critical low-frequency band. C4 and C5 have little influence at lower frequencies but reduce the phase delay at higher frequencies. C5 is not particularly useful to the CV control loop, but, has been found to enhance the stability of the constant current loop to be discussed later. A higher-frequency oscillation may result if the loop gain does not decrease sufficiently for frequencies greater than a few MHz where the phase delay rapidly increases. The small signal transfer function of the transistor network and the LT6233 gain and phase plot (Fig. 5) indicate that there should be no high-frequency oscillations.

Figure 6 is a plot of the calculated pass transistor collector current in response to a step change of the load current for the optimised component values as shown in Fig. 2 and for C2 = 100 pF. The importance of the phase lead created by C2 is evident. The influence of an input voltage ripple was simulated by adding a 4 V_{p-p}

500 Hz sinewave (V5) to the 35 V input source (V1). The output voltage ripple is 13 μV_{p-p} for a load current of 2 A and negligible for a load current of 10 mA.

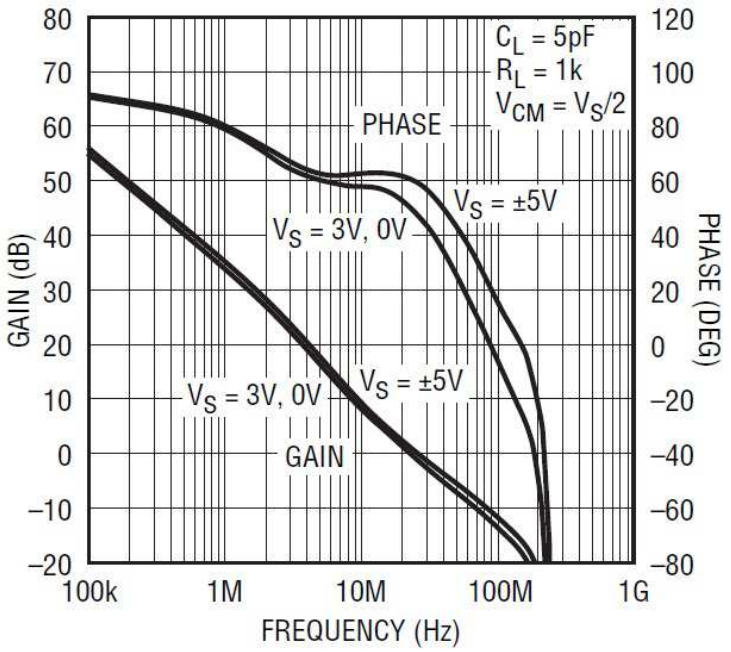

Figure 5: Open-loop gain and phase of the LT6233 opamp.

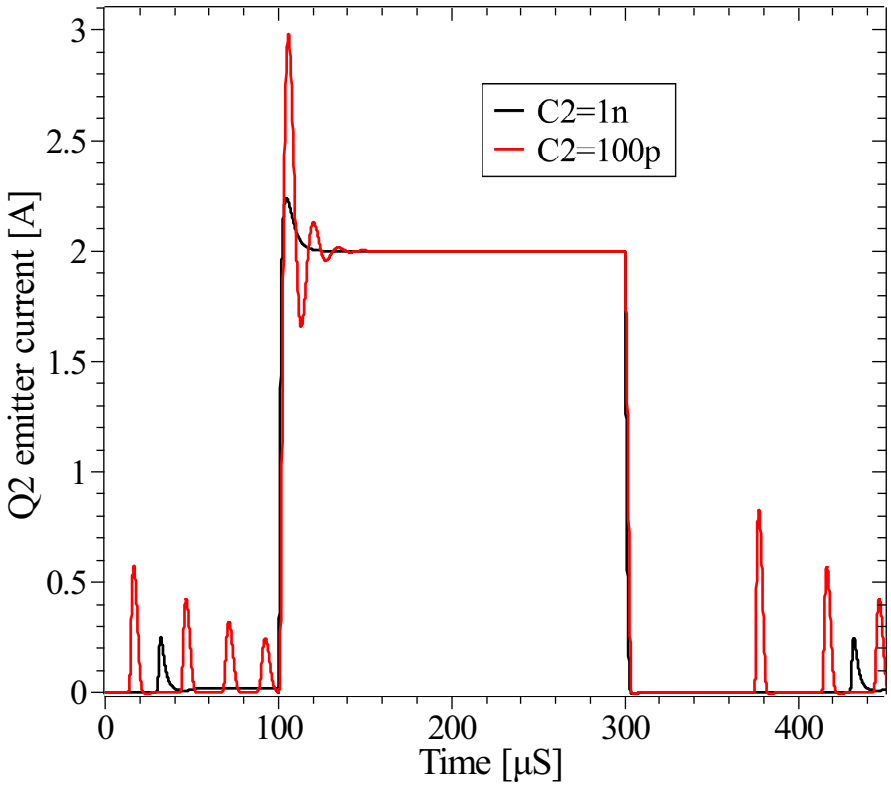

Figure 6: Simulation of the constant voltage loop response (see schematic of figure 2) to a step increase of load current from 20 mA to 2 A.

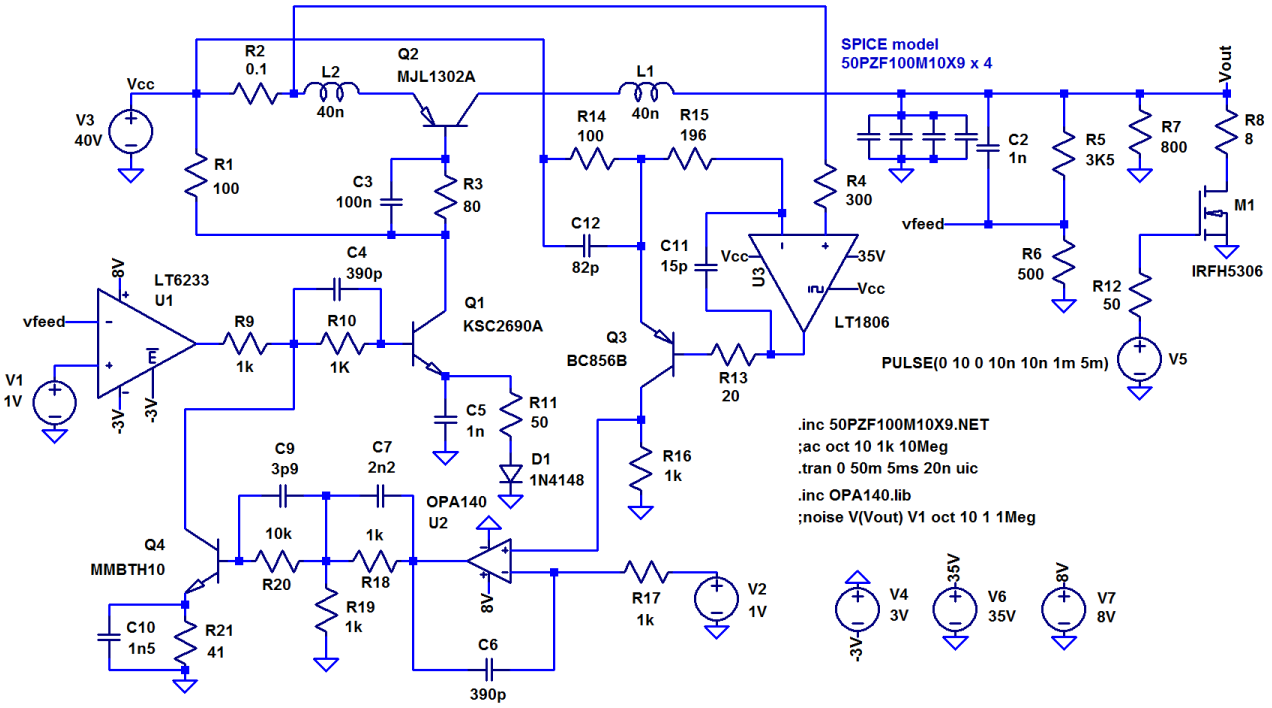

Figure 7: Schematic diagram of the CV and CC control loops as simulated by LTspice.

The full simulation schematic of the combined CV and CC control loops is shown in Fig. 7. Although the CC and CV loops share circuitry, the CC loop is compatible with optimal CV loop component values, or thereabouts. The LT1806 opamp senses the voltage across R2 and together with R14, R16 and Q3 produces a voltage across R16 in proportion to the emitter current of Q2, $\mathrm{V_{R16}} = \mathrm{I_{Q2_E}}$. LT1806 has a relatively large gain-bandwidth product of about 325 MHz such that the voltage across R16 has little phase delay in response to the emitter current of Q2 at the frequencies of importance to the entire CC feedback loop. The OPA140 opamp compares the voltage across R16 to the current limit setting voltage. When $\mathrm{V_{R16}}$ becomes greater than the current limiting voltage the MMBTH10 transistor starts to conduct and draw current away from the base of Q1. Capacitor, C6, limits the gain provided by opamp, U2, at higher frequencies and C7 together with R18 and R19 provide some phase lead in a frequency band centred at about 80 kHz. C10 provides a phase lead at frequencies greater than about 1 Mhz. The net effect is a loop gain of less than unity at the frequencies where the phase delay is greater than 360°. The OPA140 opamp has an important property; there are no protection diodes connected between the inputs and large differential voltages are permissible without input current draw. This property is important since it permits a large current limit setting voltage to be present on the inverting input of U2 without interfering with the voltage across R16, which will ultimately be used for measuring the load current. Fig. 8 displays the response of the CC circuit to a step increase of load current with current limiting set to 0.5 A. The time taken to limit current is 2 μS with a settling time of about 15 μS. Ultimately, the voltage across R16 will be measured by an ADC to indicate the load current. There is a load current measurement error due to β variations of the pass transistor, Q2, since its base current contributes to current measurement but not to the load current. The MJL1302A is very linear with respect to emitter current over the 50 mA to 4 A range but has a small early voltage, therefore the measurement error will mostly have a dependence on output voltage and transistor temperature. If the load current measurement is calibrated for a particular pass transistor gain value, β_{cal}, the relative measurement error is,

$$\frac{\Delta \mathrm{I}_{meas}}{\mathrm{I}_{meas}} = \frac{1}{\beta} - \frac{1}{\beta_{cal}} \tag{7}$$

Given the expected temperature and voltage dependence of β as indicated by the MJL1302A datasheet and its SPICE model, the maximum load current measurement error is less than 1.0% over the supply voltage and a pass transistor temperature of 25 to 100°C. With knowledge of Q2 characteristics this error can be corrected by software, to a degree. Another consequence of the early voltage of Q2, together with input voltage ripple, is output ripple current of the CC mode,

$$\mathrm{I}_{ripple} = \mathrm{I}_{load} \frac{V_{ripple}}{V_{early}} \frac{1}{\beta} \tag{8}$$

The above equation ignores the effects of the base current and early voltage of Q3, which will tend to correct the base current error and ripple current contribution of Q2. For an input ripple of 4 V_{p-p} the load current ripple predicted by SPICE simulations is 0.18 mA_{p-p} for a load current of 1A.

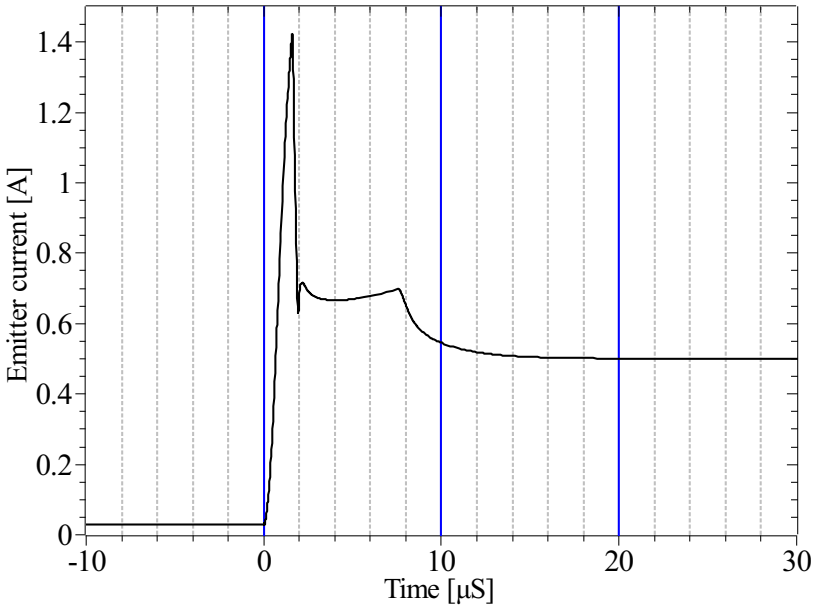

Figure 8: Simulated constant current loop response (see schematic of figure 7) to a step increase of load current.

3 Analog prototype board

The analog sections of the power board were prototyped and characterised. The prototype schematic diagram and PCB layout are shown in figures 10 - 12. The prototype schematic closely matches the SPICE simulation circuit, with the addition of opamp and reference voltage power circuitry. The prototype board was populated and characterised with the component values as shown in the schematic diagram. Careful consideration has (and must) be given to the PCB layout in order for the circuit to behave as intended. A substandard layout will degrade performance from optimal. The PCB layout can have an impact upon the following LPS characteristics in particular,

- Load regulation
- Ripple
- Excessive transient ringing / stability issues

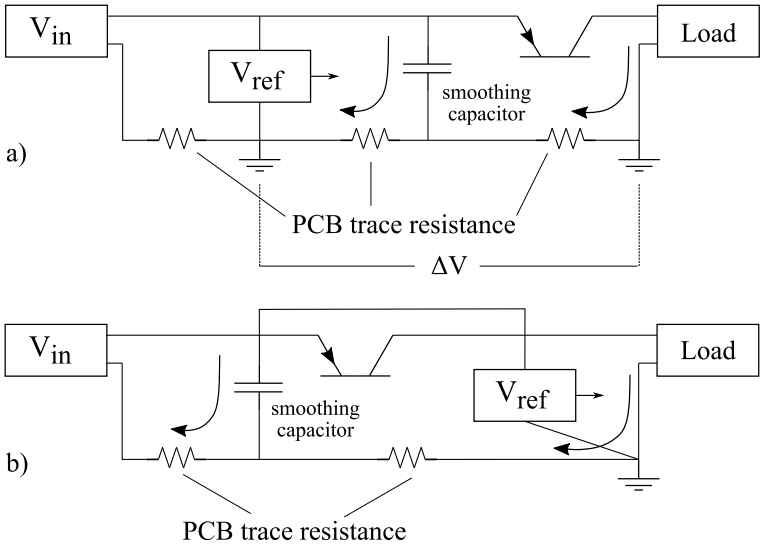

Figure 9: Diagram of a) poor PCB layout resulting in excess ripple due to current loops and b) the strategy used to minimise excess ripple.

Ground current loops can result in ripple and degraded voltage regulation as demonstrated in Fig. 9. Fortunately, the effects of ground current loops are easily minimised by following two strategies. All large currents, namely those associated with the input, filtering capacitors and the output load are isolated from the control loops. In addition, the point at which the control loop reference voltages derive their ground potential is taken at the output connector. Optimising the PCB layout in regards to transient response requires more thought. Consideration must be given to the effects of PCB parasitic capacitance, capacitive coupling and electromagnetic coupling. Parasitic capacitance can degrade phase margin and therefore stability and capacitive and magnetic coupling can result in unintentional feedback which can lead to stability issues. Minimising the size of large current loops and providing a good ground plane for the sensitive analog sections can be very effective at reducing the effects of electromagnetic coupling.

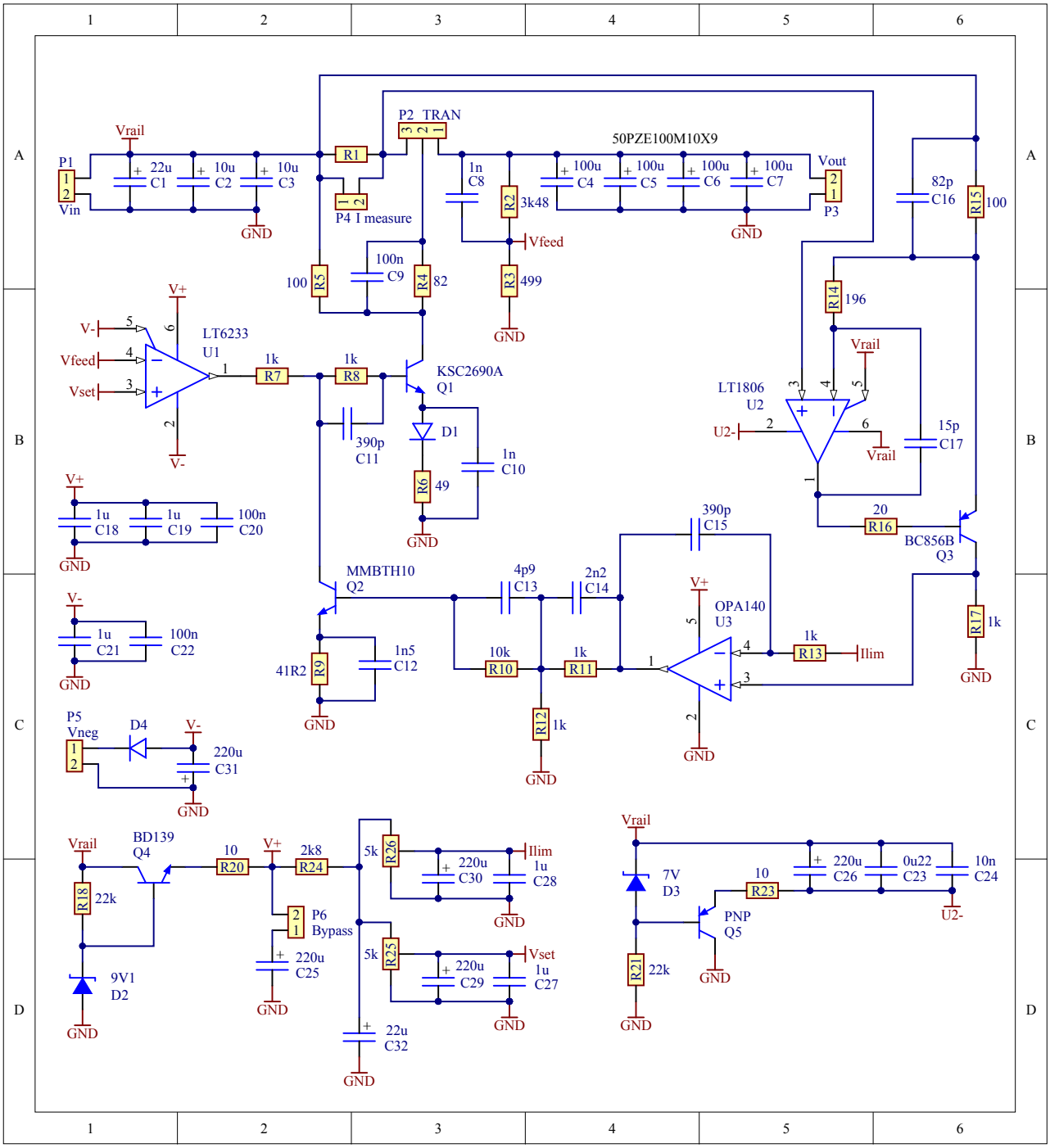

Figure 10: Schematic diagram of the analog prototype board displaying those values of the constructed circuit.

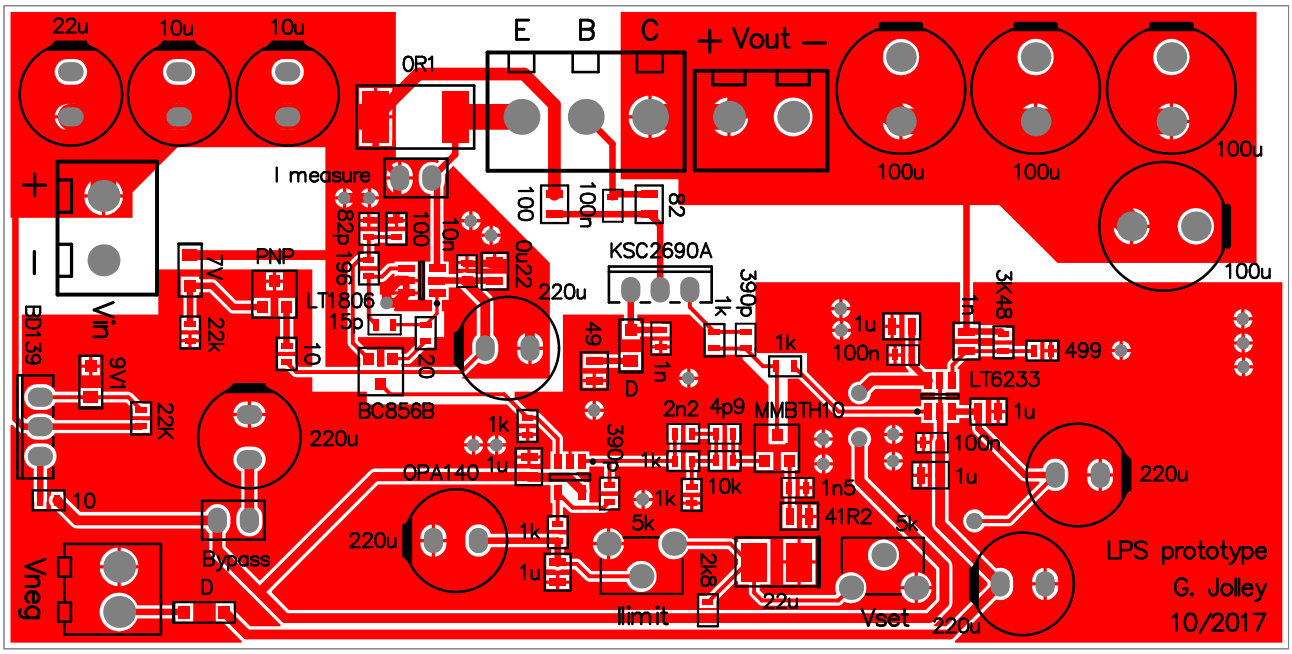

Figure 11: Top copper layer of the analog prototype PCB.

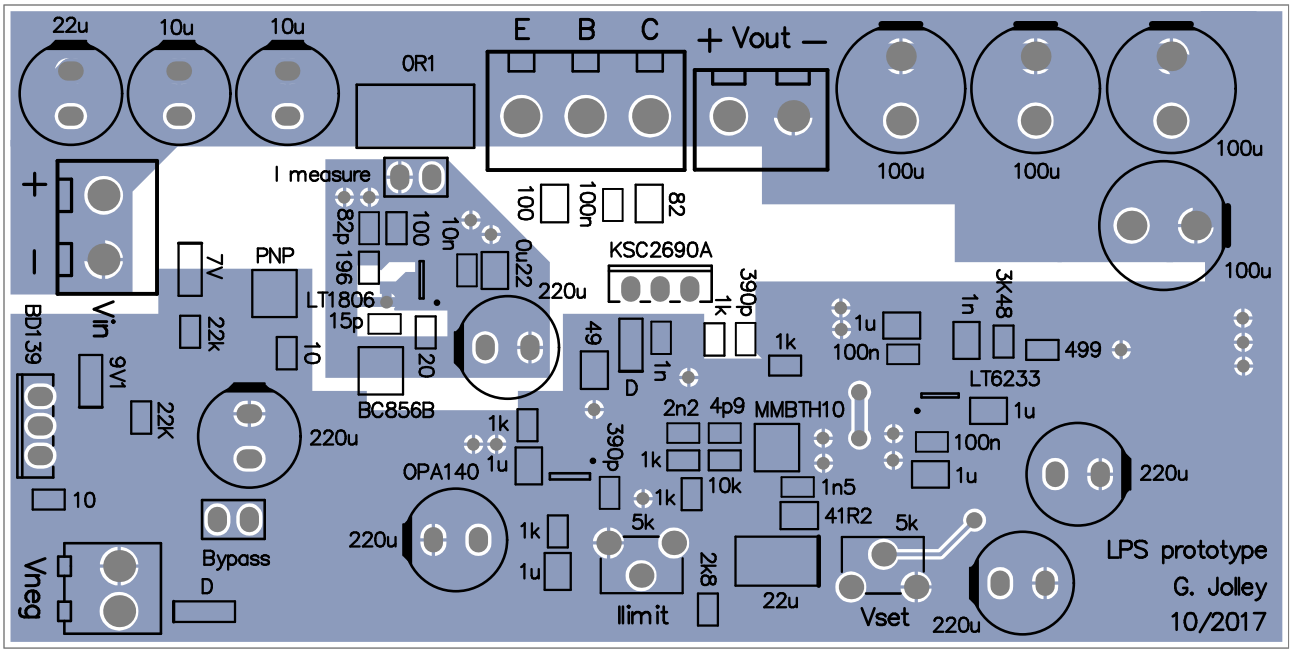

Figure 12: Bottom copper layer of the analog prototype PCB.

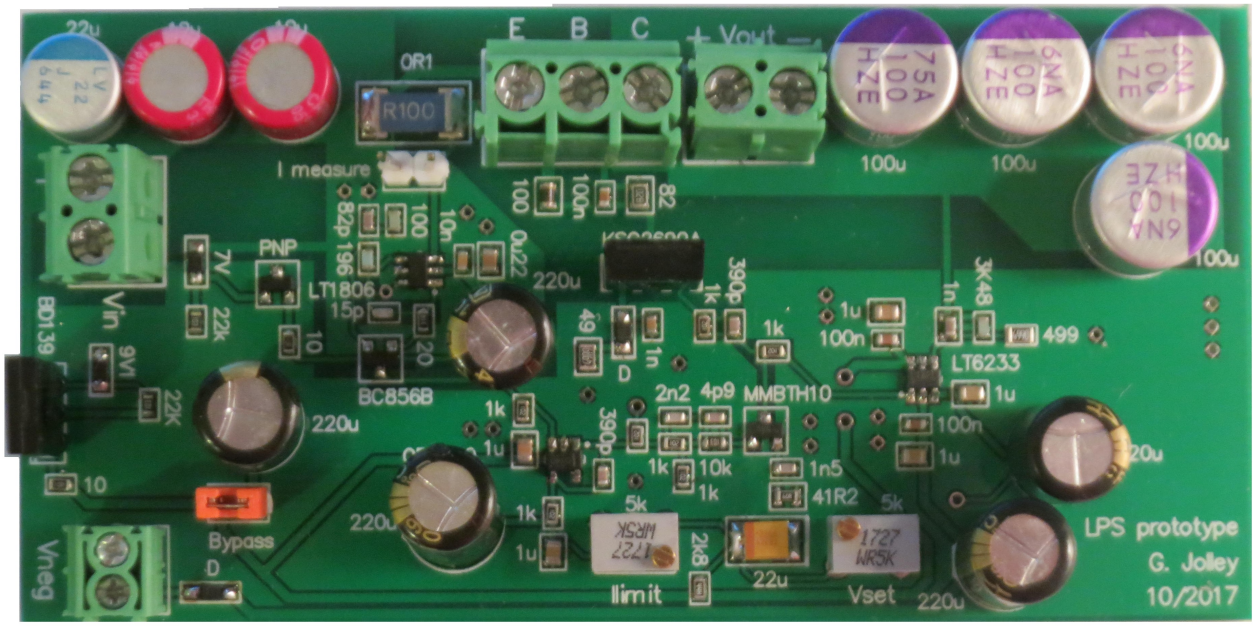

Figure 13: Constructed prototype board.

4 Analog prototype board characterisation

4.1 Transient response

A circuit switching a 10 Ω load resistor by a MOSFET with rise and fall times of about 40 nS was used to characterise the transient response of the CV mode to a rapidly changing load current. The pass transistor emitter current was captured by an oscilloscope (Digilent Analog Discovery 2) measuring the voltage across the 0.1 Ω sense resistor. The results for a step increase of load current from 20 mA to 2 A is shown in figure 14. The measured transient response agrees well with simulation showing a rise time of about 2 μS, an overshoot of 15% and no ringing. In a similar manner the response of the CC loop was obtained. With the current limit set to 0.5 A and an initial load current of 0.1 A an additional resistive load was switched across the supply, results shown in figure 15. Initially, in response to the sudden load increase, the pass transistor current overshoots to 0.82 A due to the time delay associated with the CC circuit. The response of the CC loop is rapid with a current overshoot lasting about 6 μS and a settling time of 20 μS. The constant current was evaluated with limit settings as low as 1 mA and found to be stable.

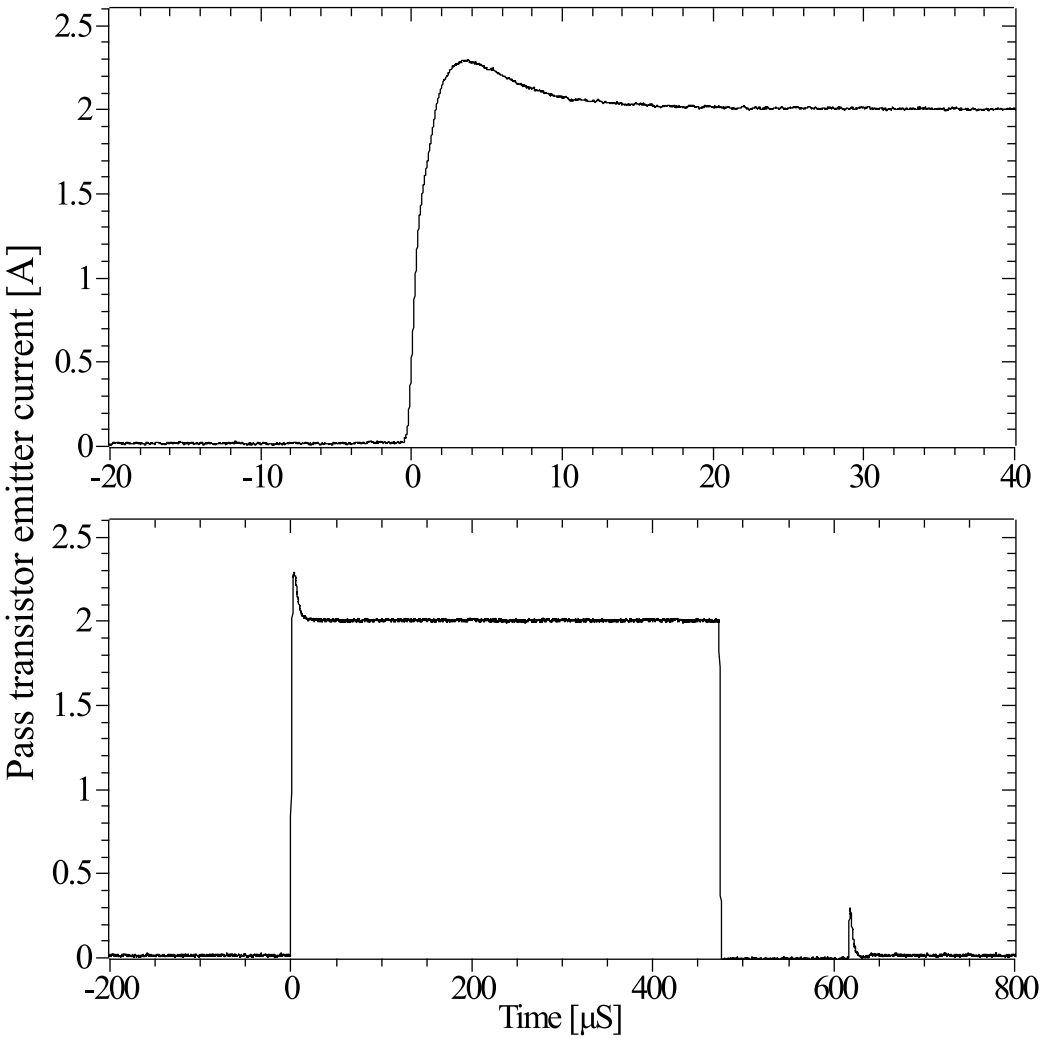

Figure 14: Measured constant voltage loop response of the prototype board to a step increase of load current from 20 mA to 2 A.

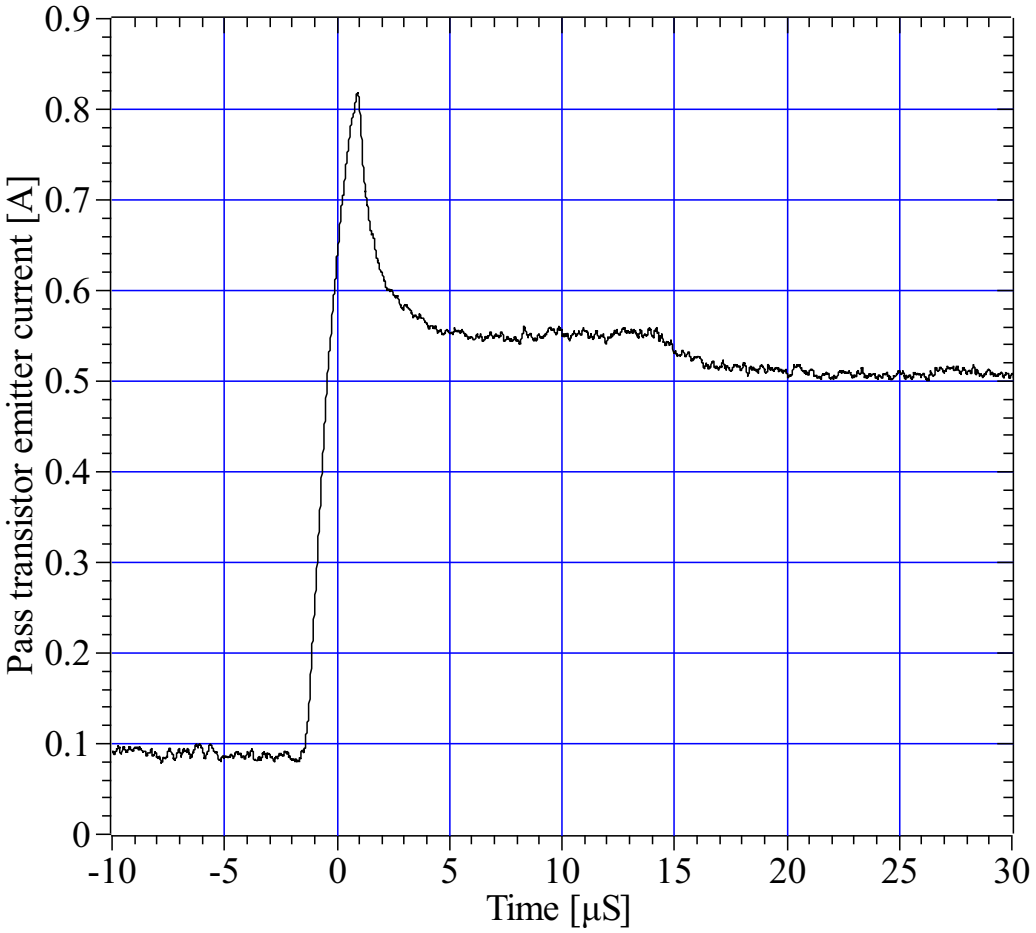

Figure 15: Measured constant current loop response of the prototype board to a step increase of load current.

4.2 Noise

Spectrum analysis result

The power supply noise within the 20 Hz - 10 kHz band was measured by connecting the output to a low-noise amplifier with a gain of 80 dB. Note, a regulated voltage source was used to power the prototype board and therefore ripple is not present in the measured results. Output noise of the CV mode was captured in the frequency and time-domain, the results of which are shown in figures 16 and 18. This result can be compared with the LTspice result shown in figure 17. There is very good agreement between the calculated, and simulated noise values. However, the measured noise spectrum is a little larger than expected for frequencies less than about 5 kHz. The discrepancy between the calculated and measured noise density has a number of possible contributions. Opamp input voltage and current noise are typically dependent on the common mode voltage, information about which is lacking in the LT6233 data sheet. Also, opamp noise figures vary from device to device. Resistor current noise has a $1/f$ dependence and is unlikely to make anything but a negligible contribute to the output noise.

Those sources of wideband noise which significantly contribute to the output voltage noise are well known and the magnitude of the noise is easily calculated. In CV mode the noise sources are:

- The voltage and current input referred noise of opamp U1
- The thermal noise of feedback resistors R2 and R3

Noise sources within the feedback loop have minimal impact upon the output noise since the negative feedback loop minimises their influence. Referring to figure 10, the output voltage noise density at flat band frequencies greater than about 1 kHz is calculated to be,

$$\frac{R2+R3}{R3}\left[\mathrm{e_n^2}+\mathrm{I_n^2}\left(\frac{R_2R_3}{R_2+R_3}\right)^2+4k_BT\frac{R_2R_3}{R_2+R_3}\right]^{1/2} \tag{9}$$

$$8\left[\left(1.9\times10^{-9}\right)^2+\left(7.8\times10^{-13}\times438\right)^2+438\times4\times1.38\times10^{-23}\times300\right]^{1/2}\ \mathrm{V}/\sqrt{\mathrm{Hz}} \tag{10}$$

$$=26.5\,\mathrm{nV}/\sqrt{\mathrm{Hz}} \tag{11}$$

This value is very must less than the upper specification limit of 158 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$. The voltage and current noise of the LT6233 opamp increases for frequencies less than 1 kHz and 100 Hz respectively.

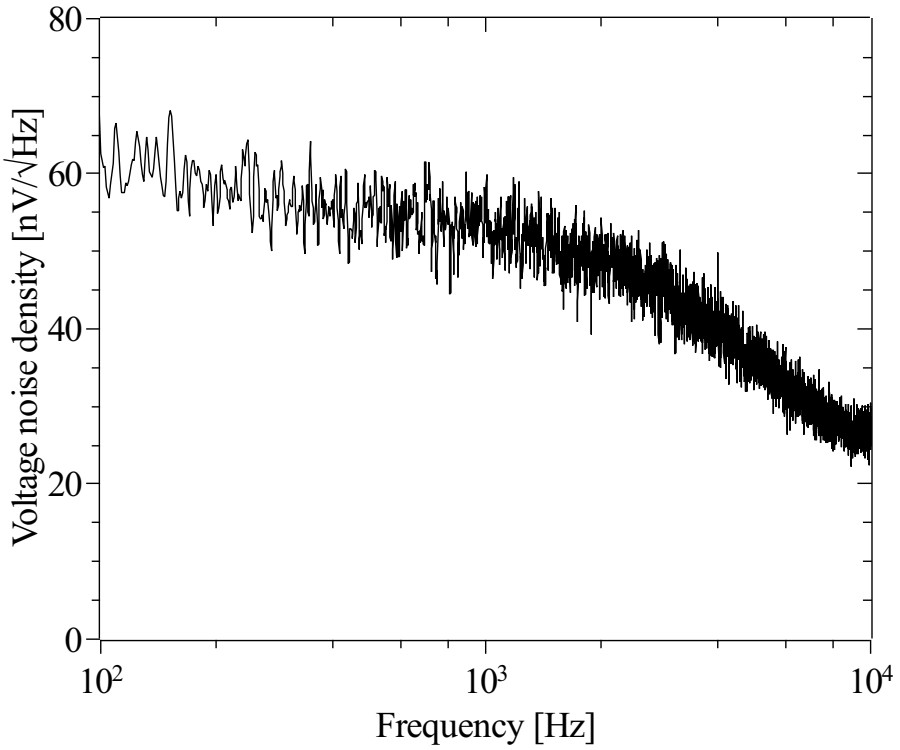

Figure 16: Measured output voltage noise spectrum, CV mode.

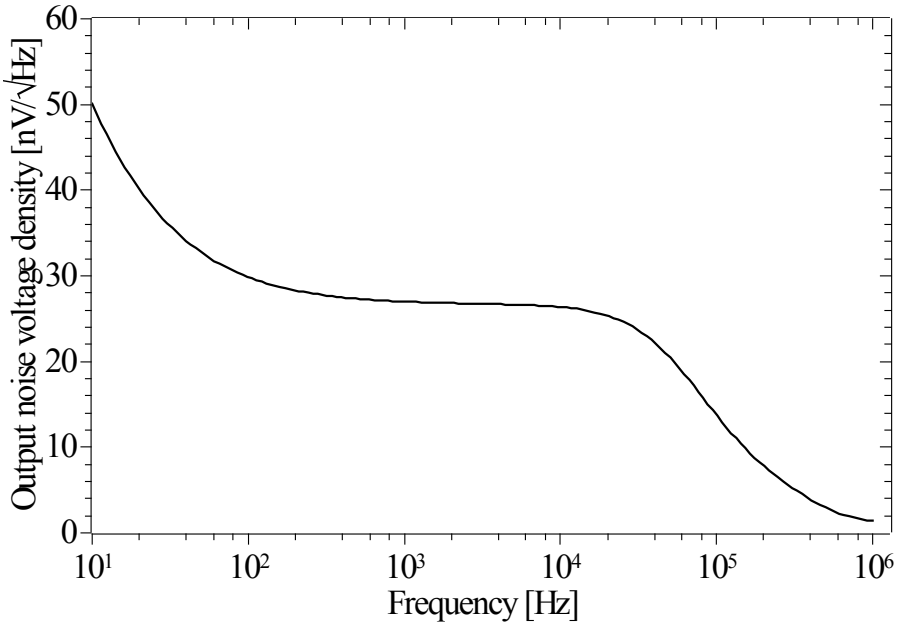

Figure 17: Simulated output voltage noise spectrum of the CV loop.

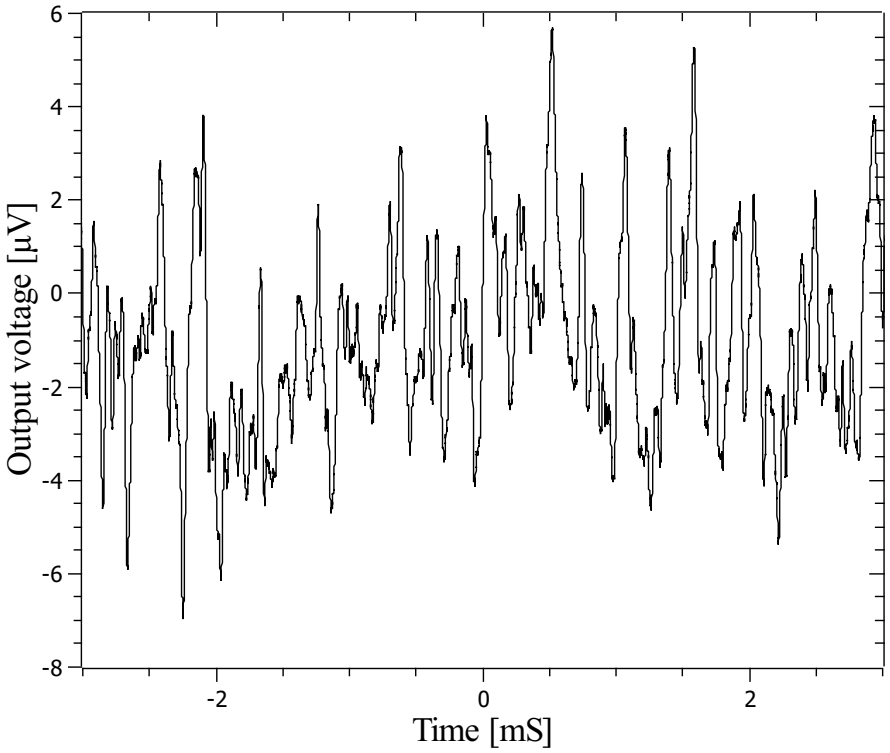

Figure 18: Measured output voltage noise within the 10-10 kHz band, CV mode.

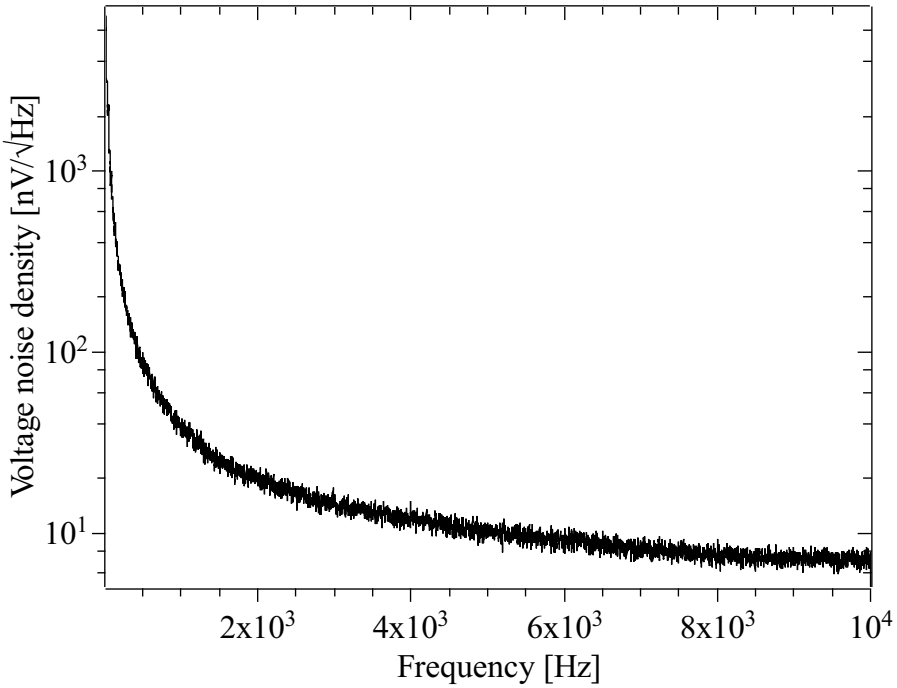

Figure 19: Measured output voltage noise spectrum, CC mode.

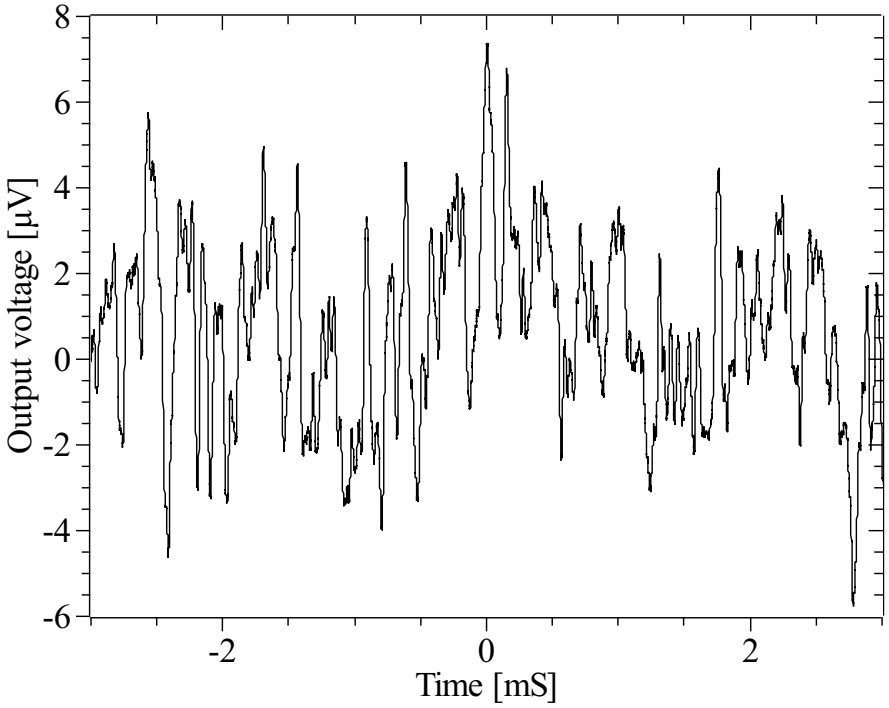

Figure 20: Measured output voltage noise within the 10-10 kHz band, CC mode.

5 Low-voltage power board

The low-voltage power board utilizes an NPN pass transistor topology which has the advantage of a dramatic reduction of the base current error that the PNP pass topology exhibits. I was also motivated by an interest in experimenting with the NPN pass topology which, generally, has a greater region of stability due to the smaller emitter impedance of the NPN pass transistor compared with PNP pass collector. The schematic diagram of the CV and CC control loops as simulated by LTspice is shown in figure 21. The base current of Q2 contributes to the current passing through the sense resistor R7 via Q1. Therefore, the load current measurement error due to β variations of the pass transistor is significantly less than that of the PNP topology of the main power board. An understanding of the CV control loop dynamics is better understood by examining SPICE simulations of the transistor network shown in figure 22, results shown in figure 23. For low frequencies the phase delay is minimal since the output appears resistive. The phase rapidly decreases and reaches a minimum somewhere from 500 Hz to 10 kHz depending on the load resistance. The decrease of the phase is partly due to R8 and C6 and the effect of the output capacitance. R8 and C6 are counter productive to the CV loop but provide stability to the CC loop. The smaller impedance of the emitter-follower and output capacitors that appear somewhat inductive result in only a small phase delay at 10 Mhz. The small signal AC gain is greater for smaller load resistances since Q2 and Q1 carry a larger base current which reduces the dynamic impedance of the base-emitter pn junction. For large load impedances, the phase delay of the CV transistor network at about 1 kHz is detrimental to stability of the CV loop unless an opamp is used that has a phase delay significantly less than the usual 90°. The LT1221 opamp is only stable for gains greater than 4 (partially decompensated) and has a phase delay significantly less than 90° for frequencies less than 10 kHz, see figure 24 for a plot of the gain and phase of the LT1221 opamp. The net results is the gain and phase margin plot of the entire CV loop as shown in figure 25.

The constant current control loop of the low-voltage supply is quite similar to that of the main supply circuit. The LT1806 opamp, U1, senses the voltage across R7 and together with R9, R11 and MOSFET Q4 produces a voltage across R11 in proportion to the emitter current of Q2, $V_{R11} = I_{Q2_E}$. LT1806 has a relatively large gain-bandwidth product of about 325 MHz such that the voltage across R11 has little phase delay in response to the emitter current of Q2 at the frequencies of importance to the entire CC feedback loop. The LT1222 opamp, U3, compares the voltage across R11 to the current limit setting voltage. When V_{R11} becomes greater than the current limiting reference voltage the MMBTH10 transistor starts to conduct and draw current away from the base of Q1. The dynamics of the CC control loop is better understood from gain and phase calculations of the circuit shown in figure 26, results shown in figure 27. The LT1222 opamp is uncompensated and has a

large gain-bandwidth 500 MHz. C12 is an external compensation capacitor that renders the opamp unity gain stable and reduces its gain-bandwidth to about 15 MHz. The 470 pF capacitor, C8 together with R12 further reduces the gain-bandwidth to about 1 Mhz, yet there is an increase of the phase at the output of U3 (N1) at frequencies greater than 100 kHz as the impedance of C8 approaches that of R12. C9 provides an important phase lead for frequencies between 1-10 MHz, adding stability. C11 also provides a small phase lead at higher frequencies. For frequencies greater than 4 MHz the phase decreases rapidly due to the bandwidth limits of the externally compensated U3. It might appear that the huge gain of the darlington configuration of Q1 and Q2 would result in a high-frequency instability of the CC loop, however, at the higher frequencies where the phase delay begins to decrease rapidly, the gain of Q1 and Q2 is significantly less than their static gain values. Further simulation results are not provided, see the final characterisation section for LV power board results.

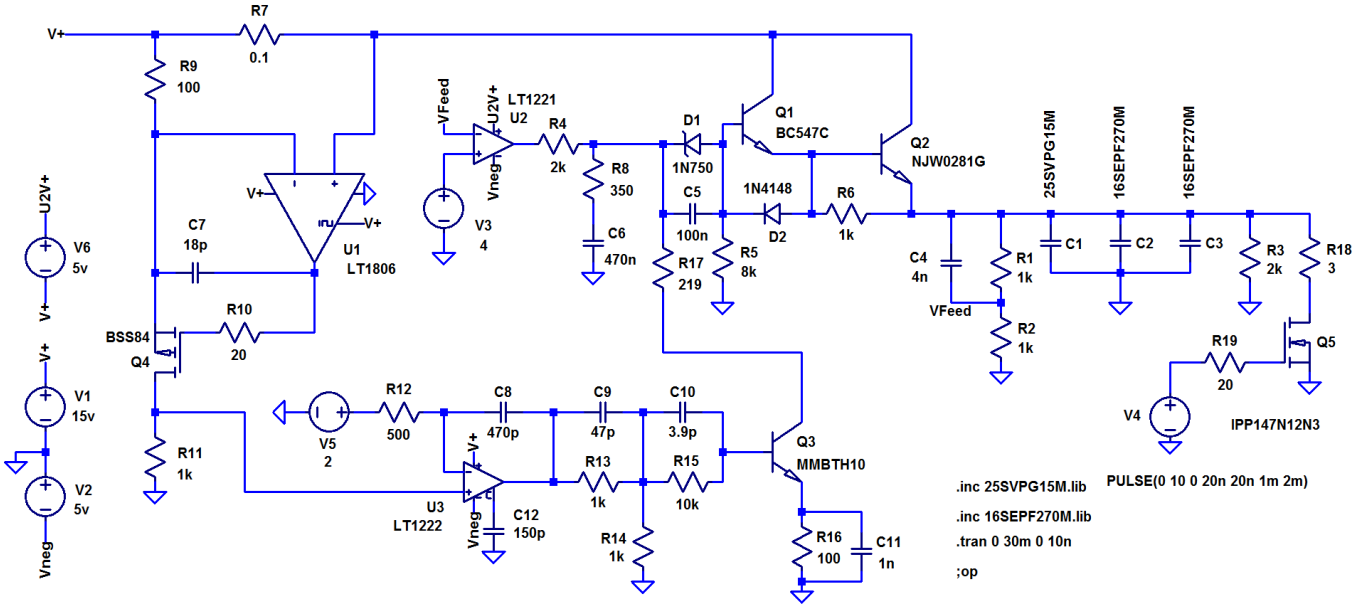

Figure 21: Schematic of the low-voltage supply as simulated by LTspice.

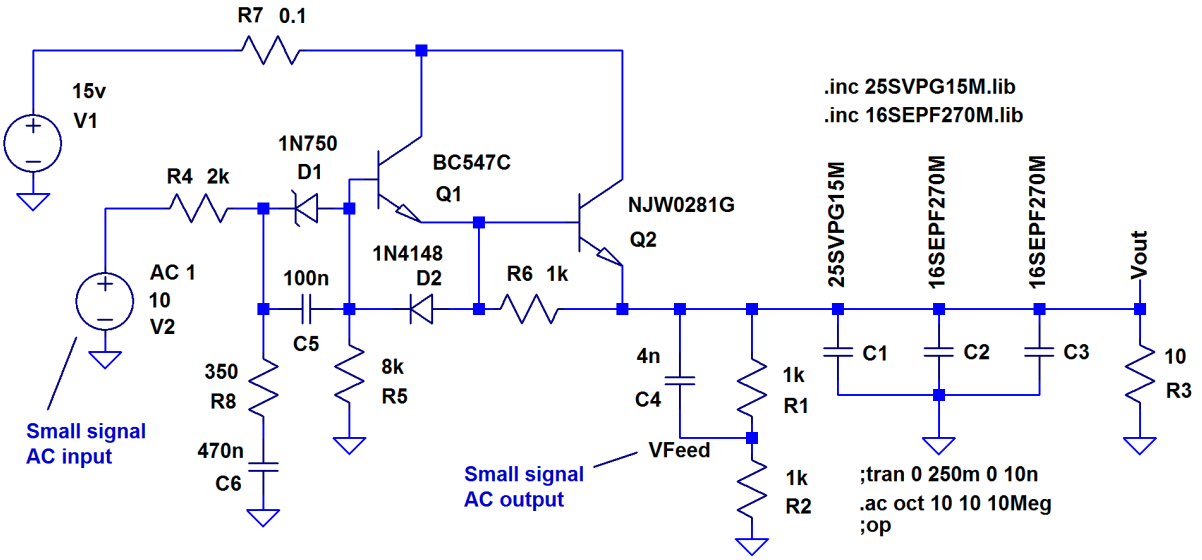

Figure 22: Transistor network of the low-voltage supply CV control loop as simulated by LTspice.

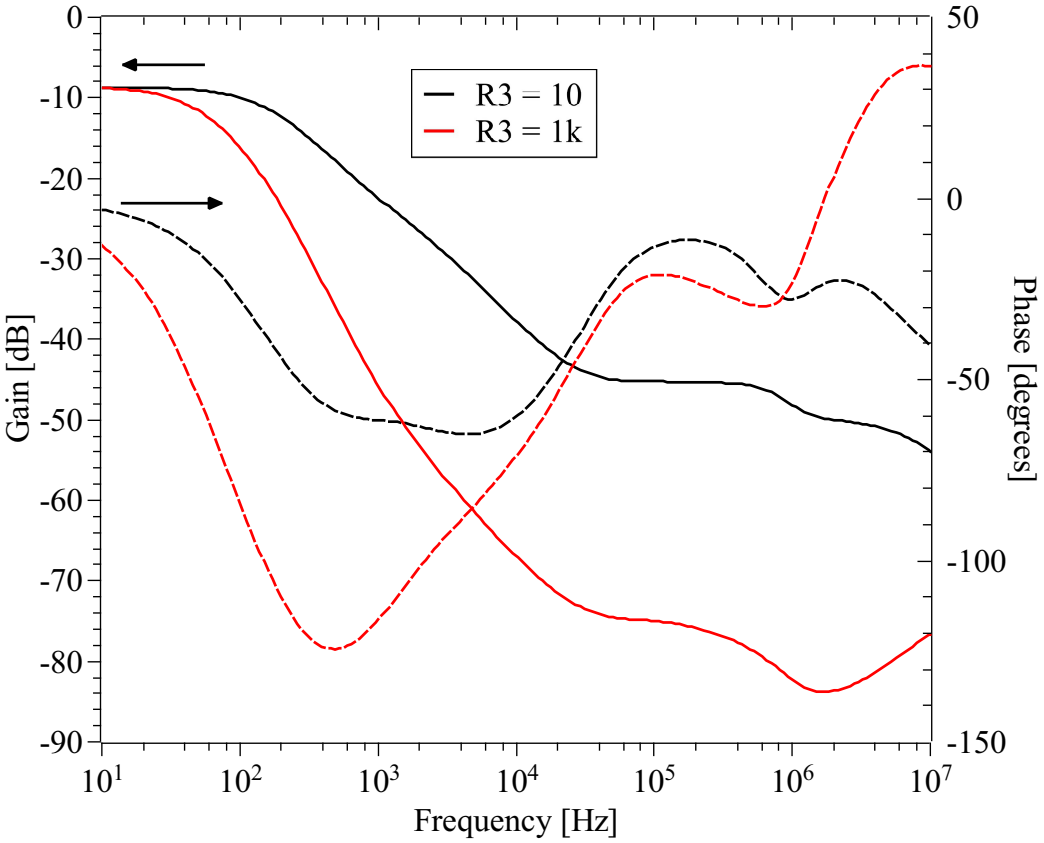

Figure 23: LTspice calculations of the phase and gain of the transistor network shown in figure 22. V2 is the AC input source and VFeed is the output. Calculations are shown for 2 different load resistances, R3 = 10 and R3 = 1k Ω.

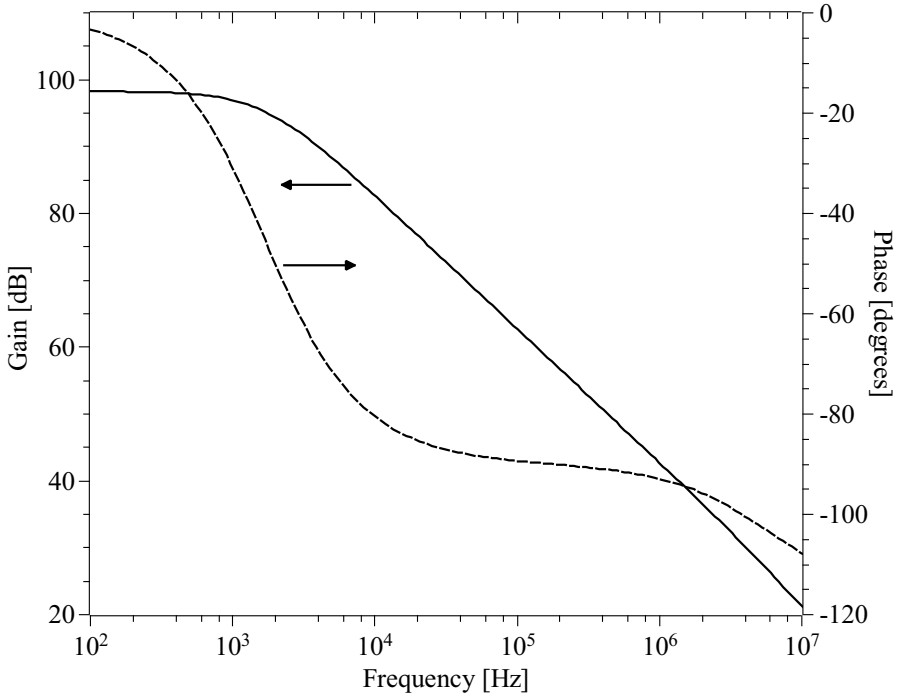

Figure 24: Phase and gain of the LT1221 opamp.

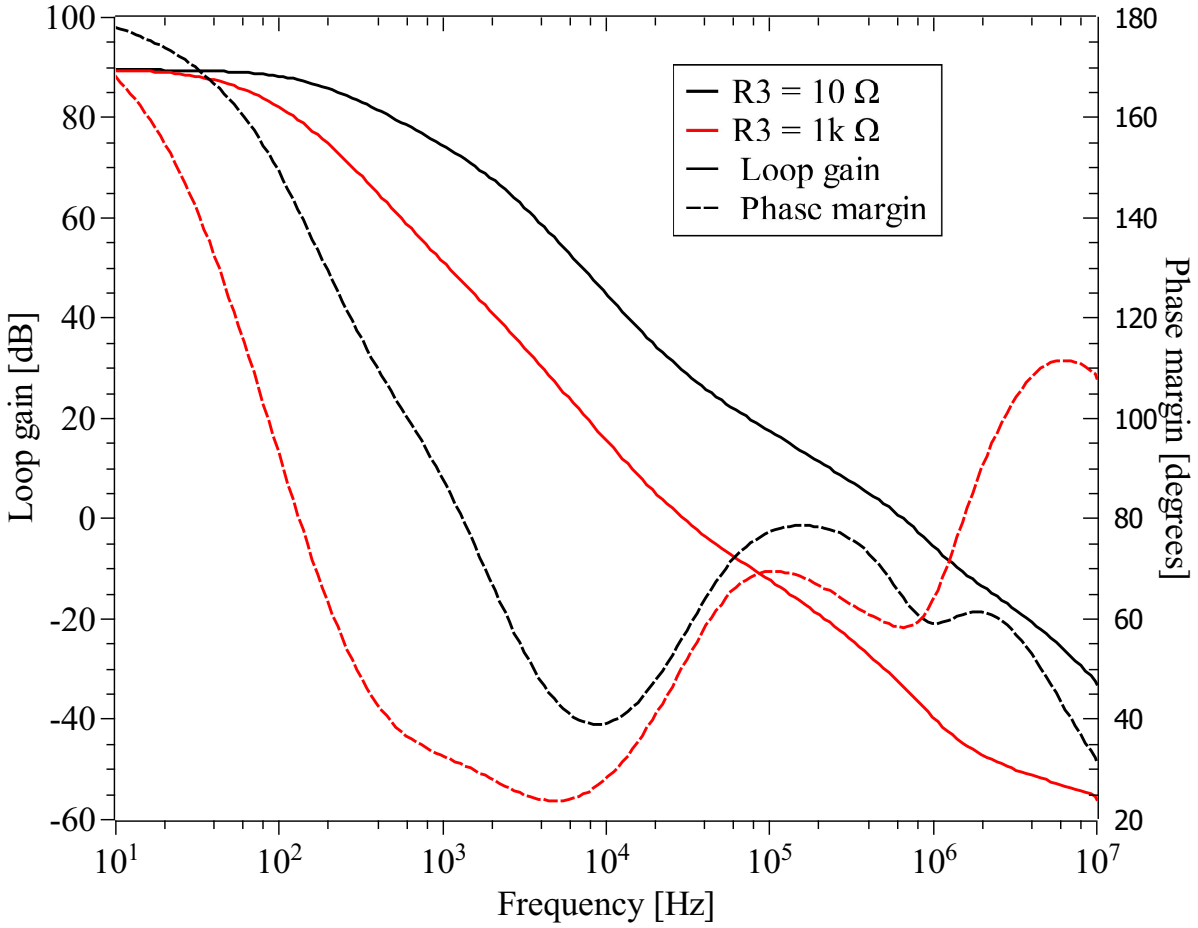

Figure 25: Gain and phase margin of the LV CV control loop.

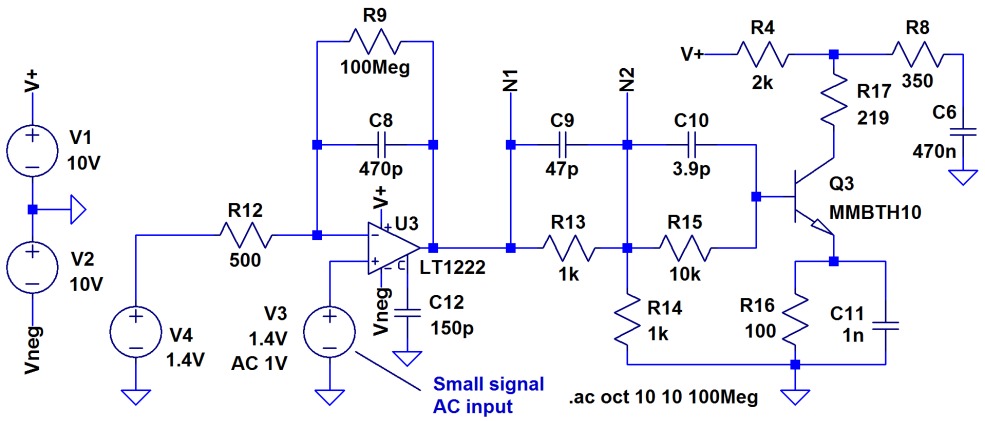

Figure 26: SPICE schematic of LT1222 opamp and some of the associated components from the CC control loop for simulation.

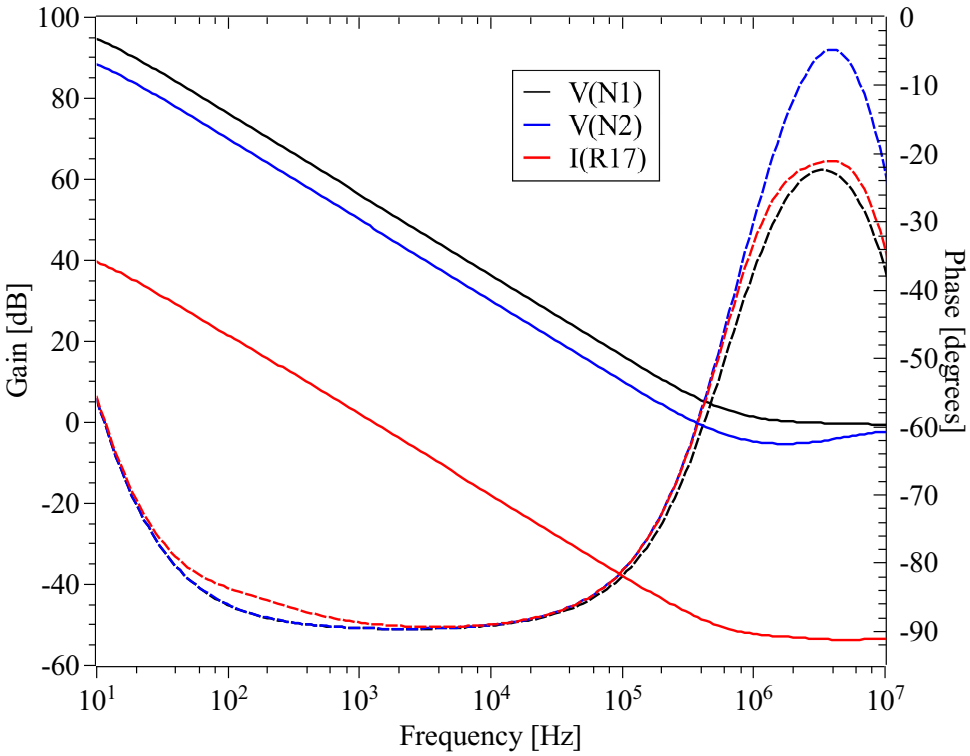

Figure 27: SPICE calculations of the gain and phase of the circuit shown in figure 26. N1, N2 and R16 are as labelled in the circuit.

6 Final schematics

6.1 Main power board

The schematic diagrams of the complete power board as constructed are shown in figures 30-32 and the PCB layout is shown in figures 33 and 34. Figure 30 displays the main CV and CC circuitry which closely follows the prototype board aside from some additional features including,

- Split-rail input voltage and associated switching circuitry
- Overcurrent digital shutdown

Each of two main power boards is powered by a 2×15V transformer which provides the split-rail 0-21-42 V_{peak} input. The split-rail input reduces the thermal dissipation of the pass transistor by only switching its emitter to the higher rail voltage when the output voltage is greater than a threshold voltage. Hysteretic switching of MOSFET Q1 ensures that it is either fully on or off. Polymer electrolytic capacitors C5-C7 provide a low impedance at higher frequency with the intention of minimising the size of the current loop between the power supply input and output. The negative supply voltage for U1 provided to connector P4 is implemented by manually winding an additional coil on the main toroidal power transformer. With the component values indicated in the schematic diagrams the maximum obtainable output voltage is 32.768 V and the maximum current limit is 4.096 A. Simulations indicate that the minimum pass transistor emitter-collector voltage is 1.8 V at the maximum load current. Such a small voltage is cutting things a bit fine and may require software limiting the maximum voltage-current product a little.

Constant current and digital shutdown protection features are implemented, the former has previously been described and characterised in the prototyping section. Each can be independently disabled by MCU control. The pass transistor emitter current produces a proportionate voltage cross R10. After low-pass filtering by a configurable RC time constant, this voltage appears on the non-inverting input of comparator U5. The comparator drives a resettable latch to shutdown transistor Q5 under load current fault conditions.

Digital control

The digital control aspects of the LPS power board are summarised as follows,

- DACs set the output voltage and current limit
- ADCs read the output voltage and load current
- A microcontroller communicates with the DACs, ADCs and control board

The LTC2641 is the chosen DAC primarily because it is unbuffered which results in a low offset error and low voltage noise density. The LTC2641 comes in 12, 14 and 16-bit resolution versions. A 16-bit part is chosen for voltage setting to allow for a 1 mV resolution. A 12-bit part is chosen for current limiting to allow for a 1 mA resolution. The ADS8866 which has 16-bits of resolution is chosen for voltage and load current readback. 16-bits of resolution is appropriate for a readback resolution of 1 mV. 16-bits of resolution allows for a load current readback of 0.1 mA, though the magnitude of the error is likely to be much greater than the resolution due to the pass transistor base current error as discussed previously, see Eq. 7.

The voltage and load current read back ADCs and the Vset and Ilimit DACs reference an external voltage source that is provided by a single 4.096 V MAX6126 that functions as a master reference. When compared with the LT6233 opamp input voltage noise of 1.9 $nV/\sqrt{Hz}$ the MAX6126 has a relatively large wideband noise specification of 80 $nV/\sqrt{Hz}$ and the DAC has an output noise density specification of 10 $nV/\sqrt{Hz}$. Therefore, filtering of the DAC output is necessary to take advantage of the very-low noise of the opamp. The following circuit is used to filter the DAC output,

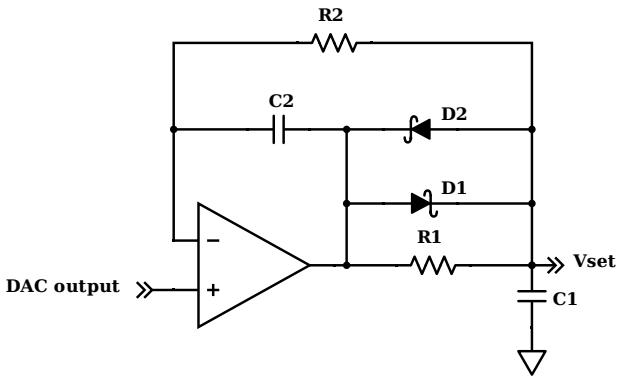

Figure 28: Reference voltage noise filter, note: $R_2C_2 = 2R_1C_1$.

The filter output slew rate is limited by the RC time constant, therefore, there is a trade-off between the settling time of Vset and the degree with which the noise is filtered. The diodes increase the maximum slew rate within the limits of their forward voltage drop. The reference filter displays overshoot to step changes of the input voltage, however, this can be mitigated with appropriate ramping of the input voltage as indicated by the LTspice simulations shown figure 29.

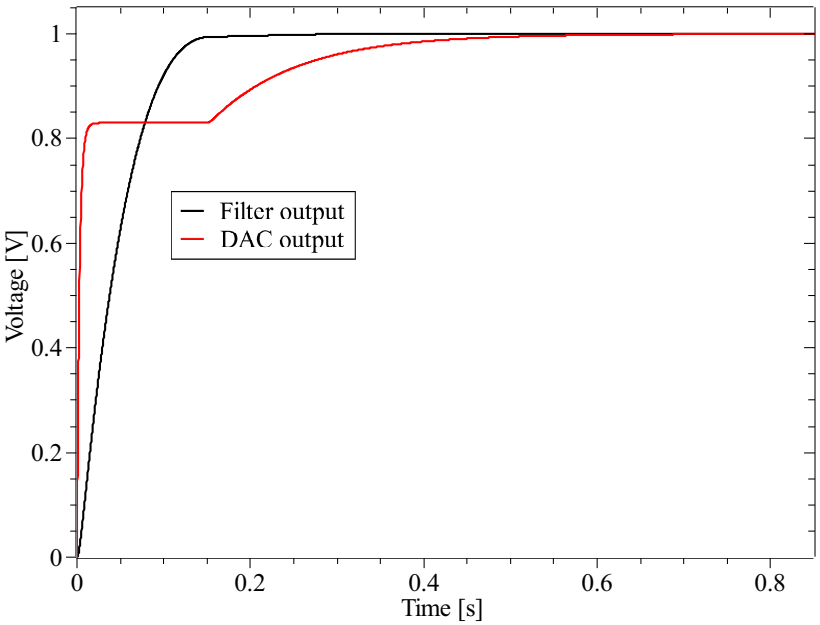

Figure 29: Reference filtering voltage ramping simulation, C1 = 47 μF, R1 = 1 kΩ.

A Si8642 isolator allows for communication with the control board with 4 unidirectional digital I/O lines, 2 are output and 2 are input. The power boards are controlled by a PIC24FJ64GA702 microcontroller which has the advantage of 3 SPI ports for communication with the ADCs, DACs and control board.

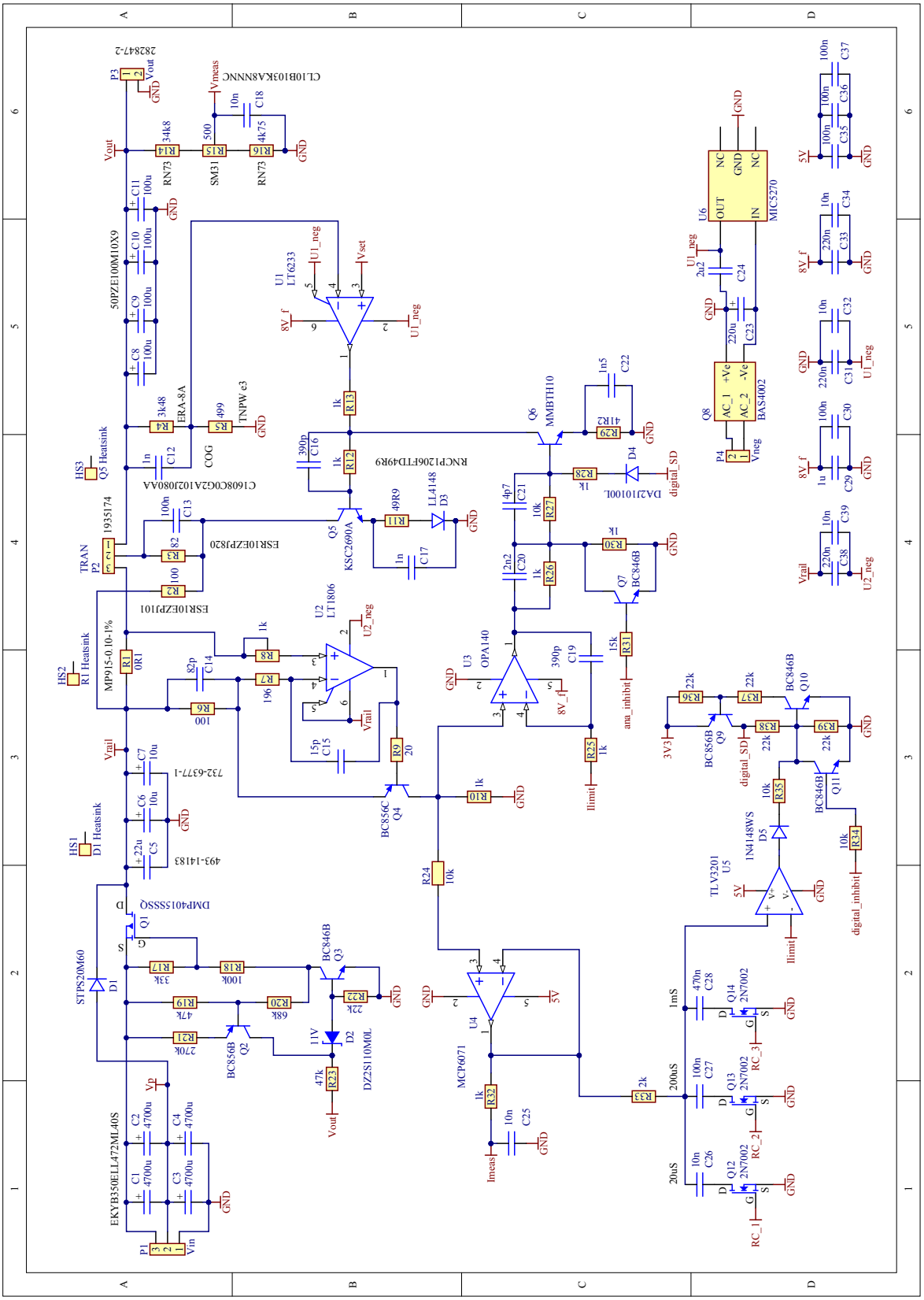

Figure 30: Main power board schematic showing the CV and CC control loops.

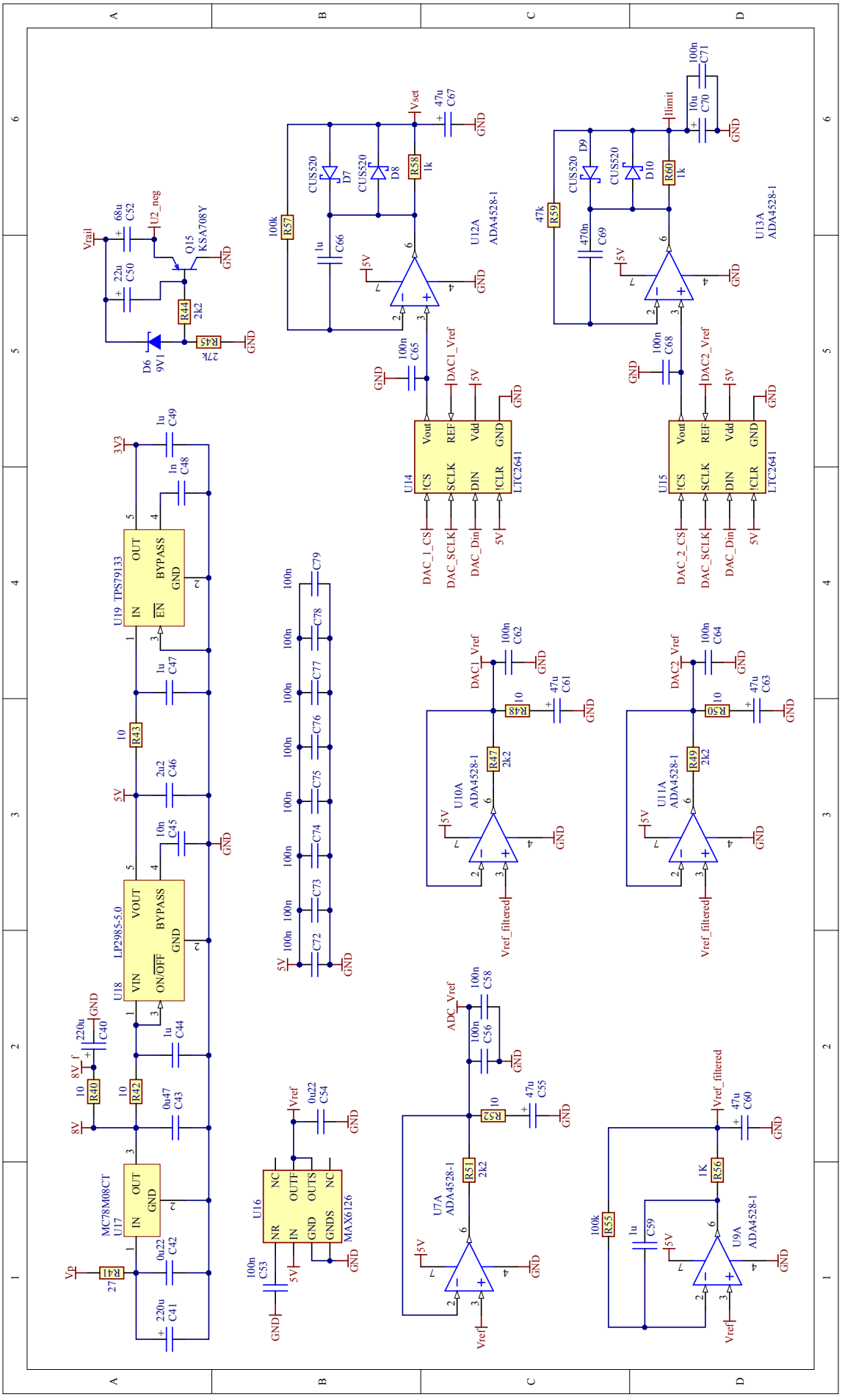

Figure 31: Main power board schematic showing reference voltage circuitry.

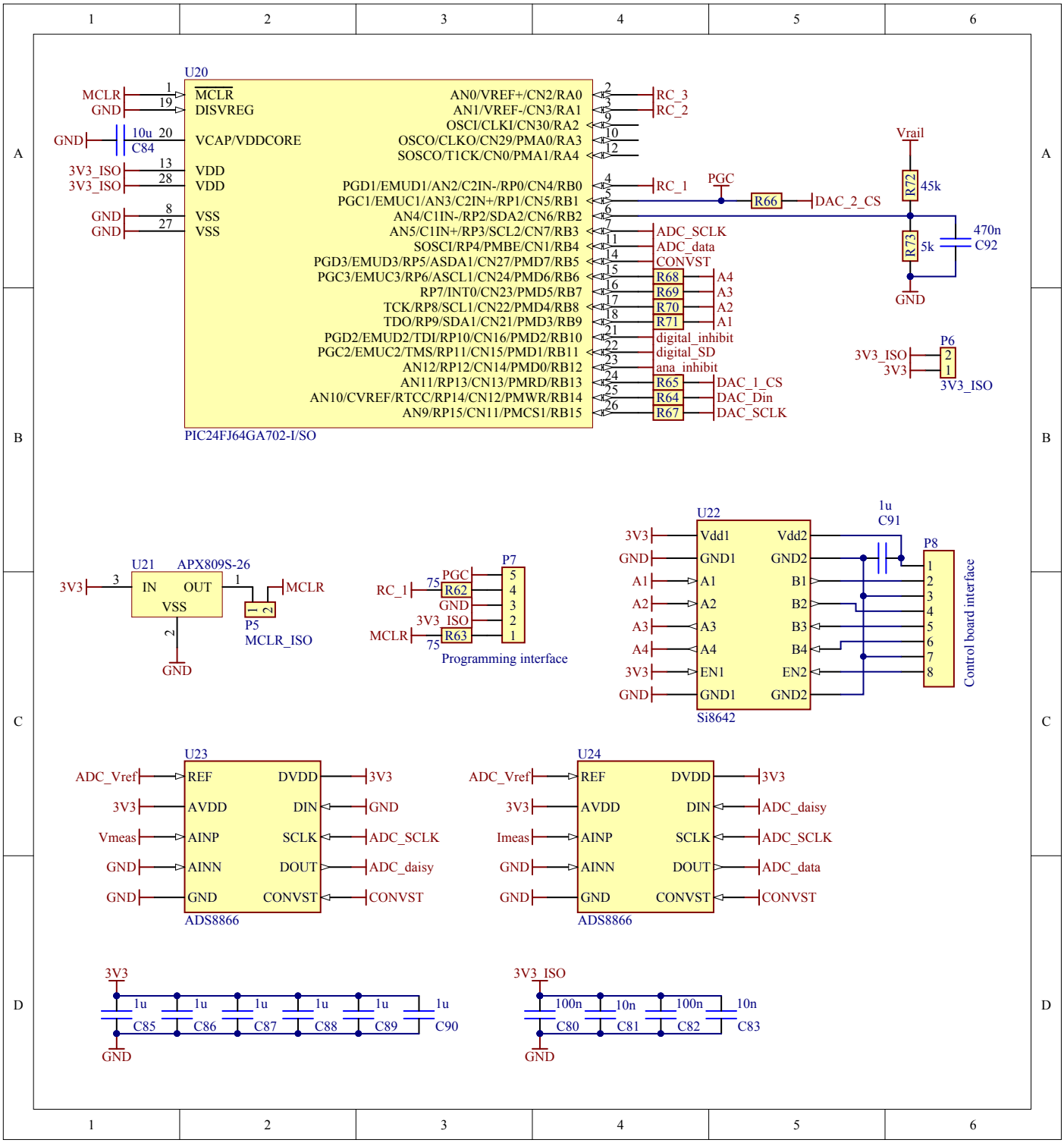

Figure 32:
Main power board schematic showing the MCU and control board communcations interface.

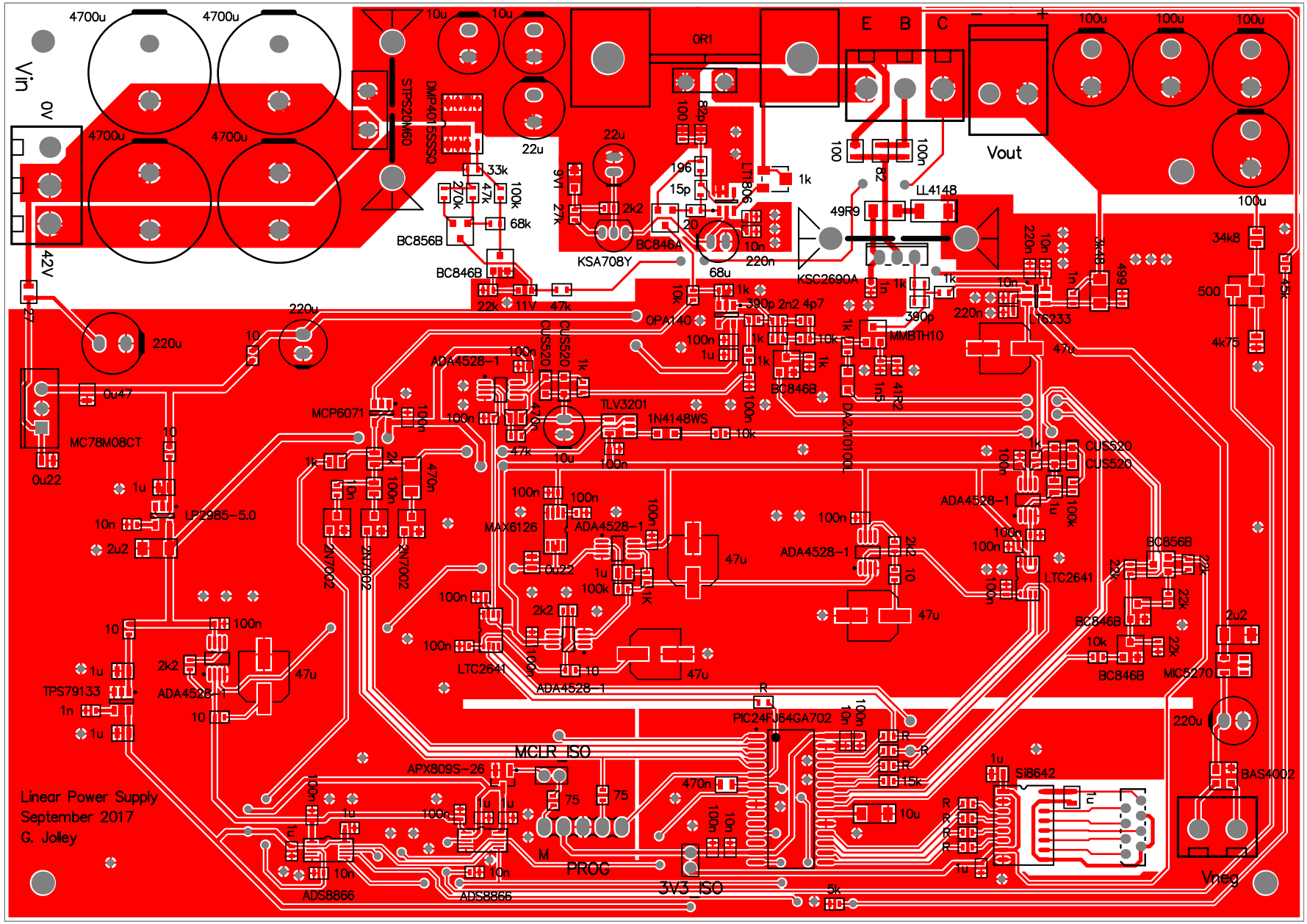

Figure 33: Main power PCB top layer

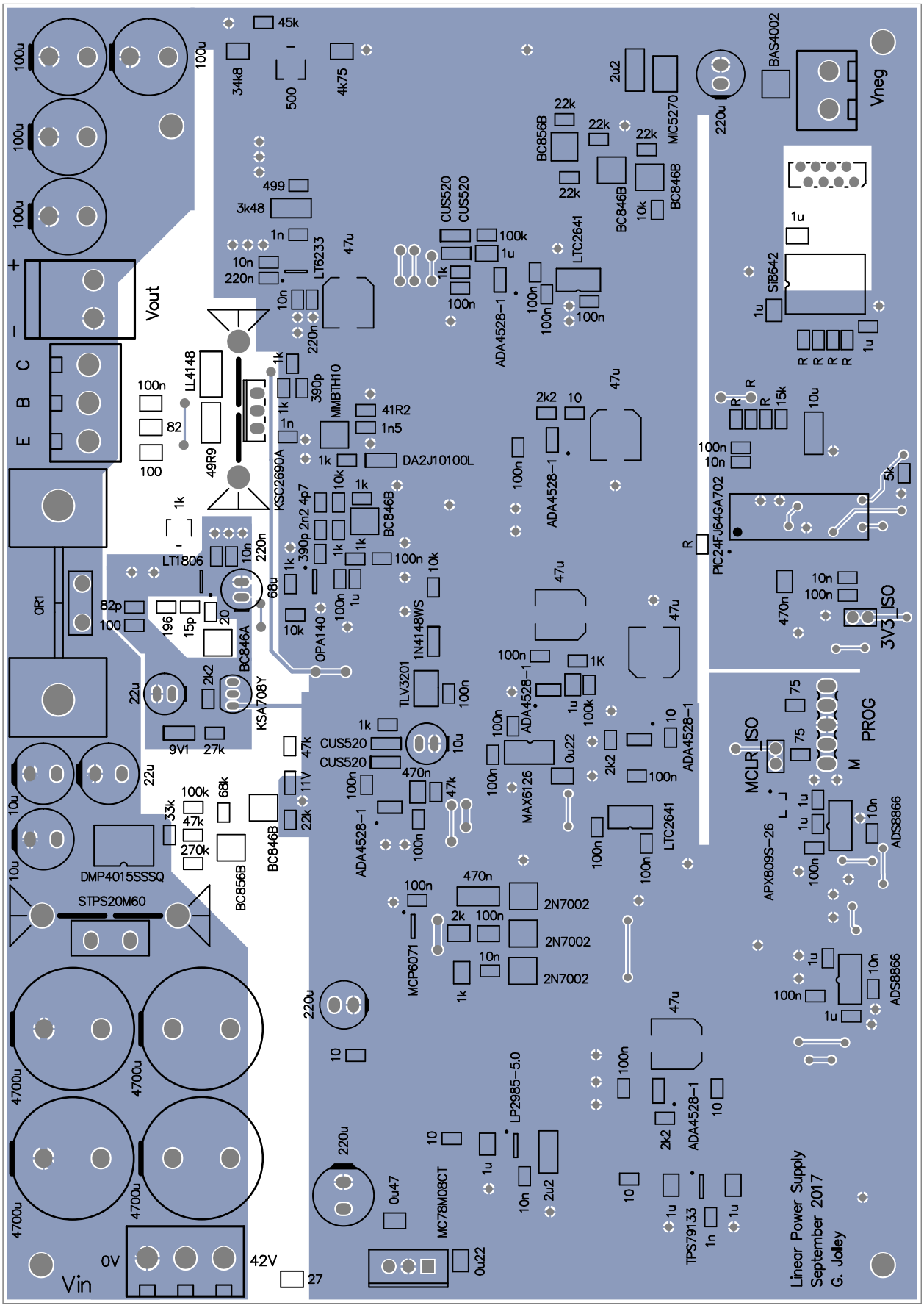

Figure 34: Main power PCB bottom layer

6.2 LV power board

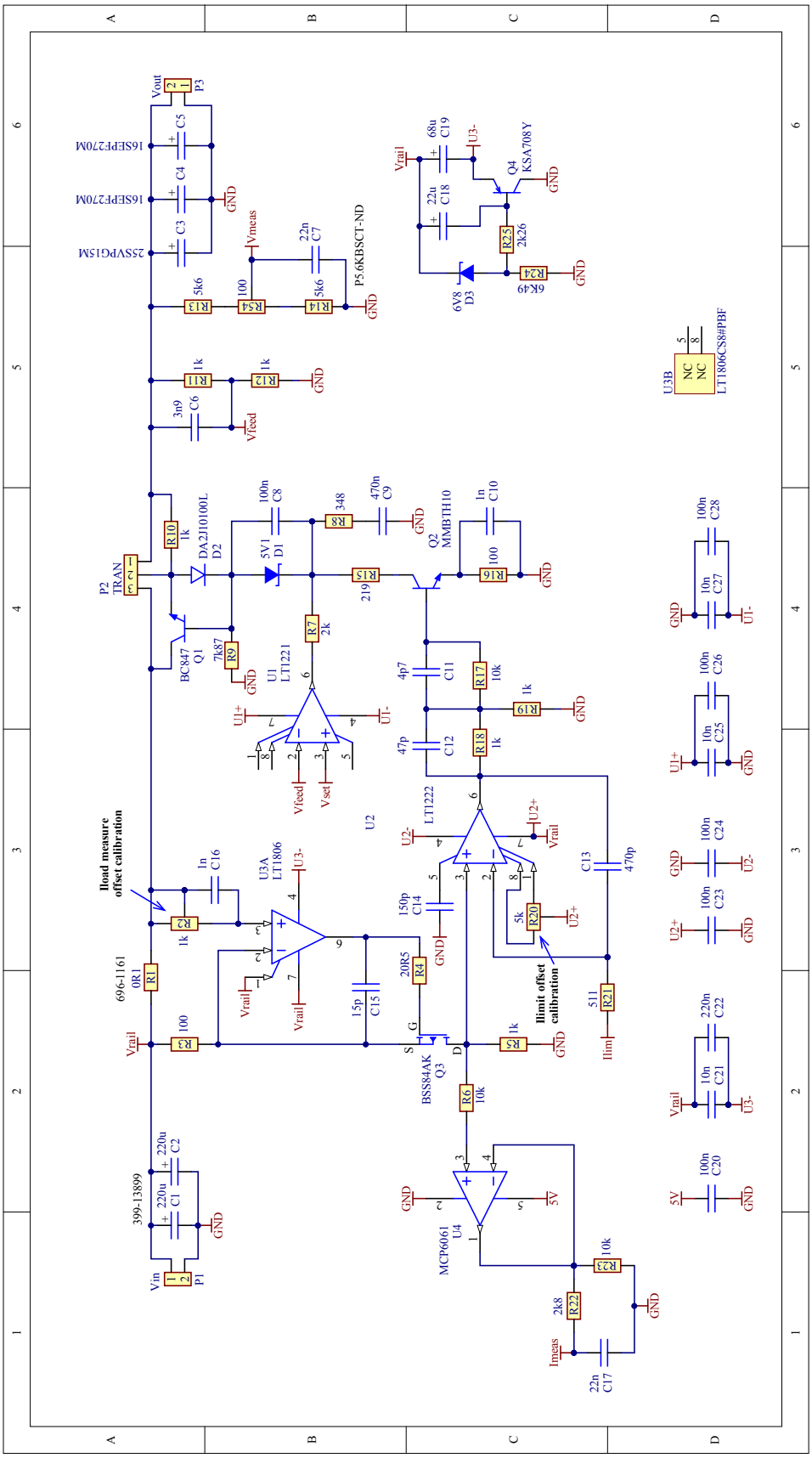

Figure 35: Low-voltage power board schematic showing the CV and CC control loops.

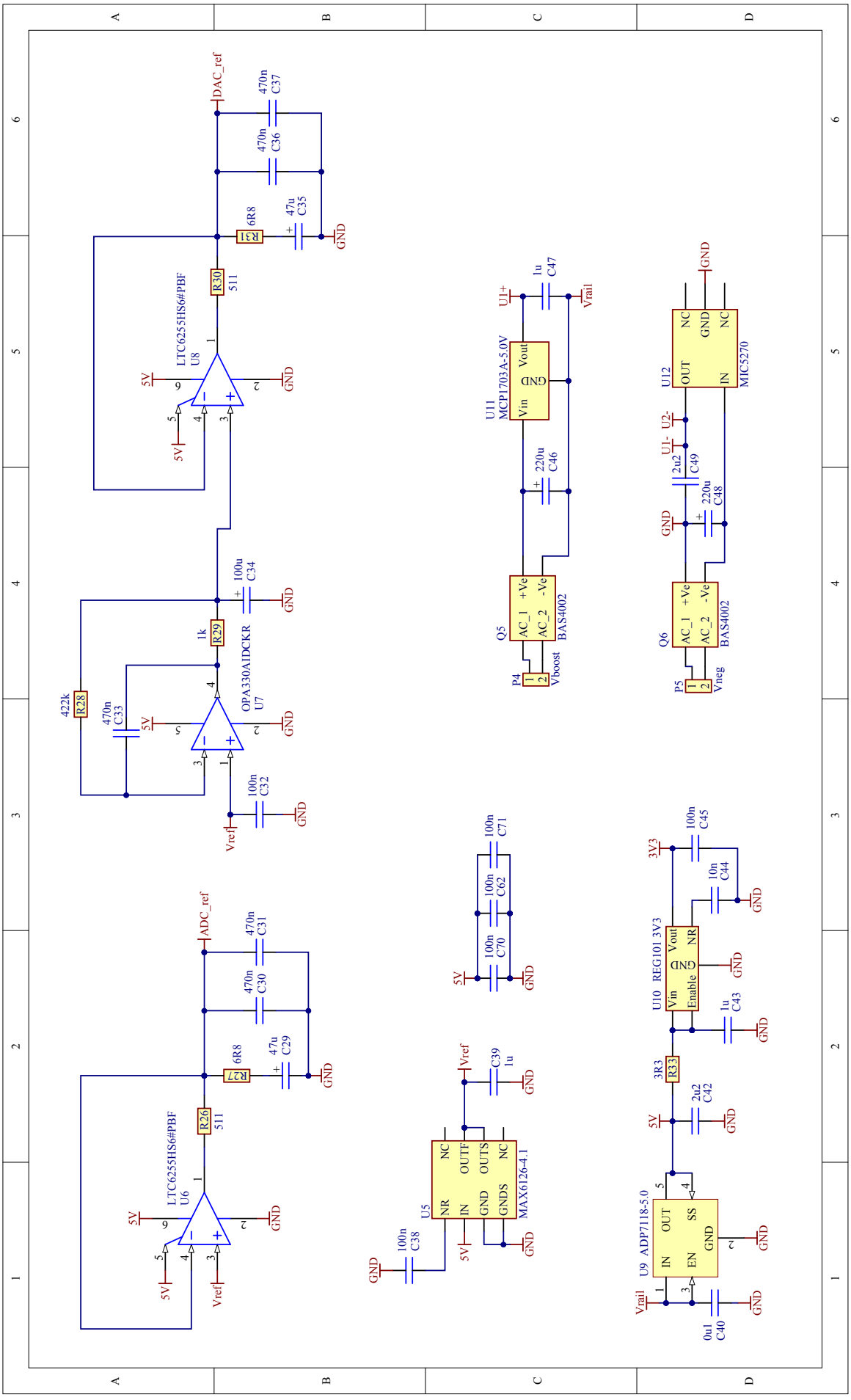

Figure 36: Low-voltage power board schematic showing reference voltage filtering.

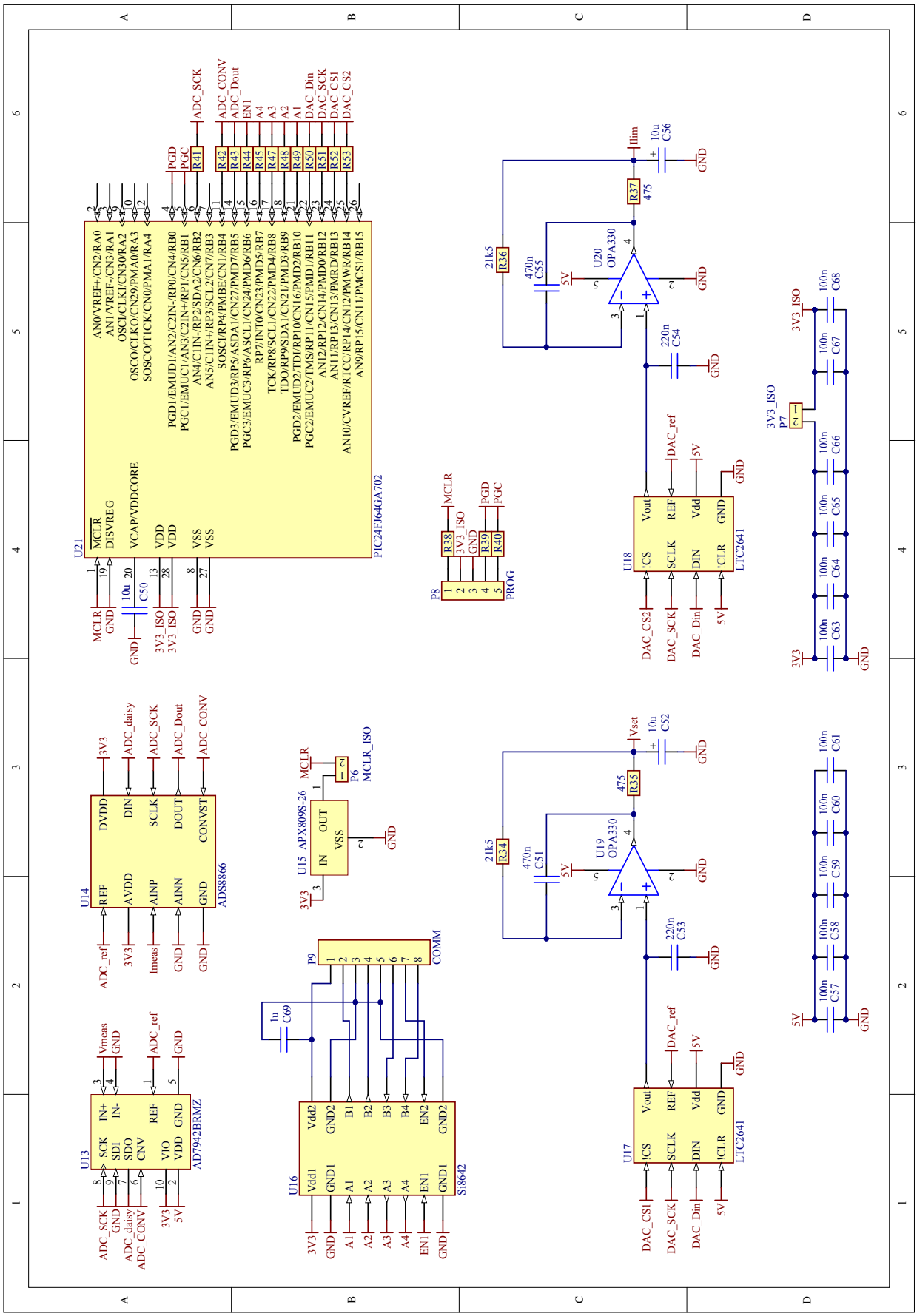

Figure 37: Low-voltage power board schematic showing MCU, ADCs and DACs.

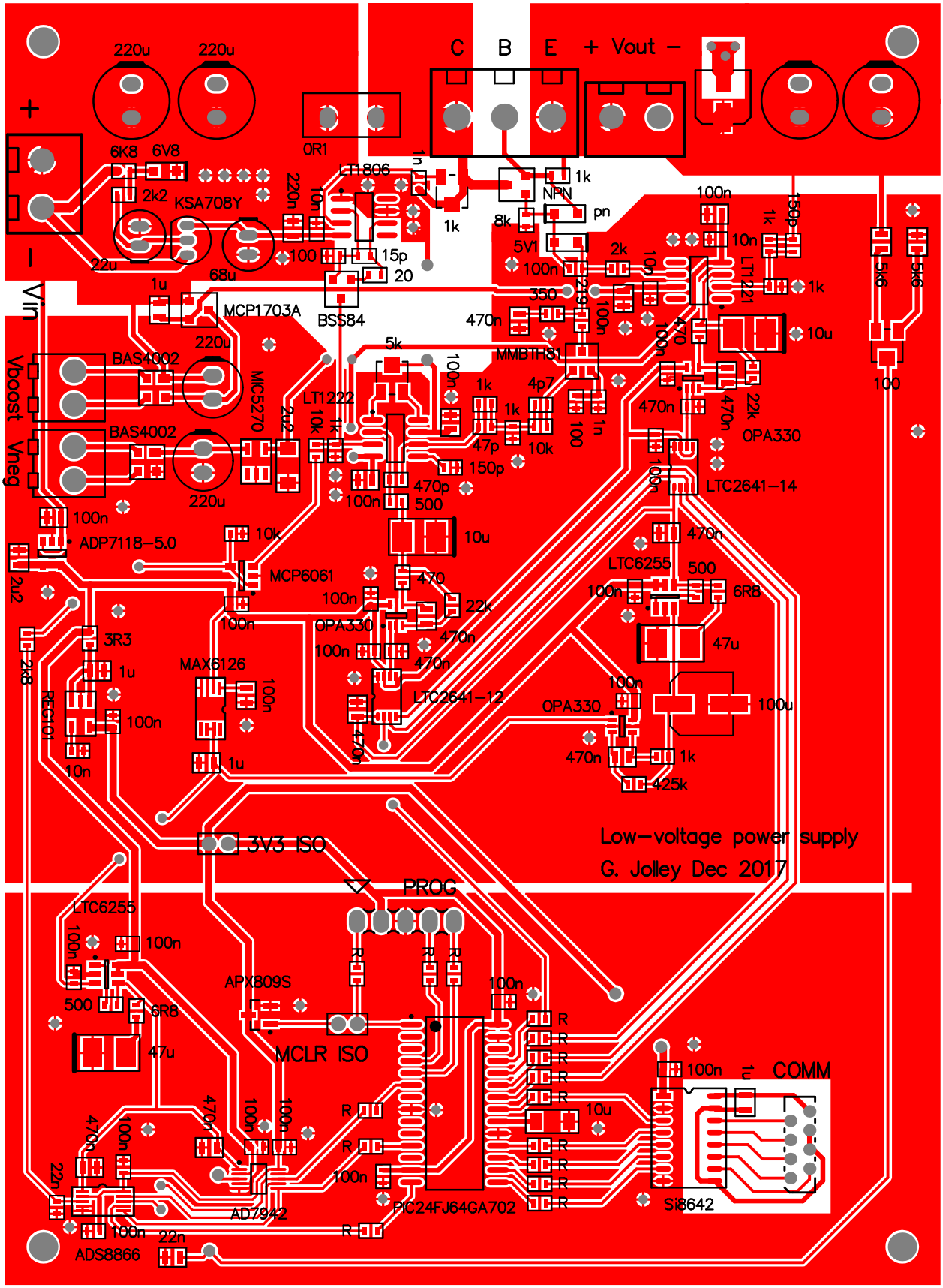

Figure 38: Low-voltage PCB top layer.

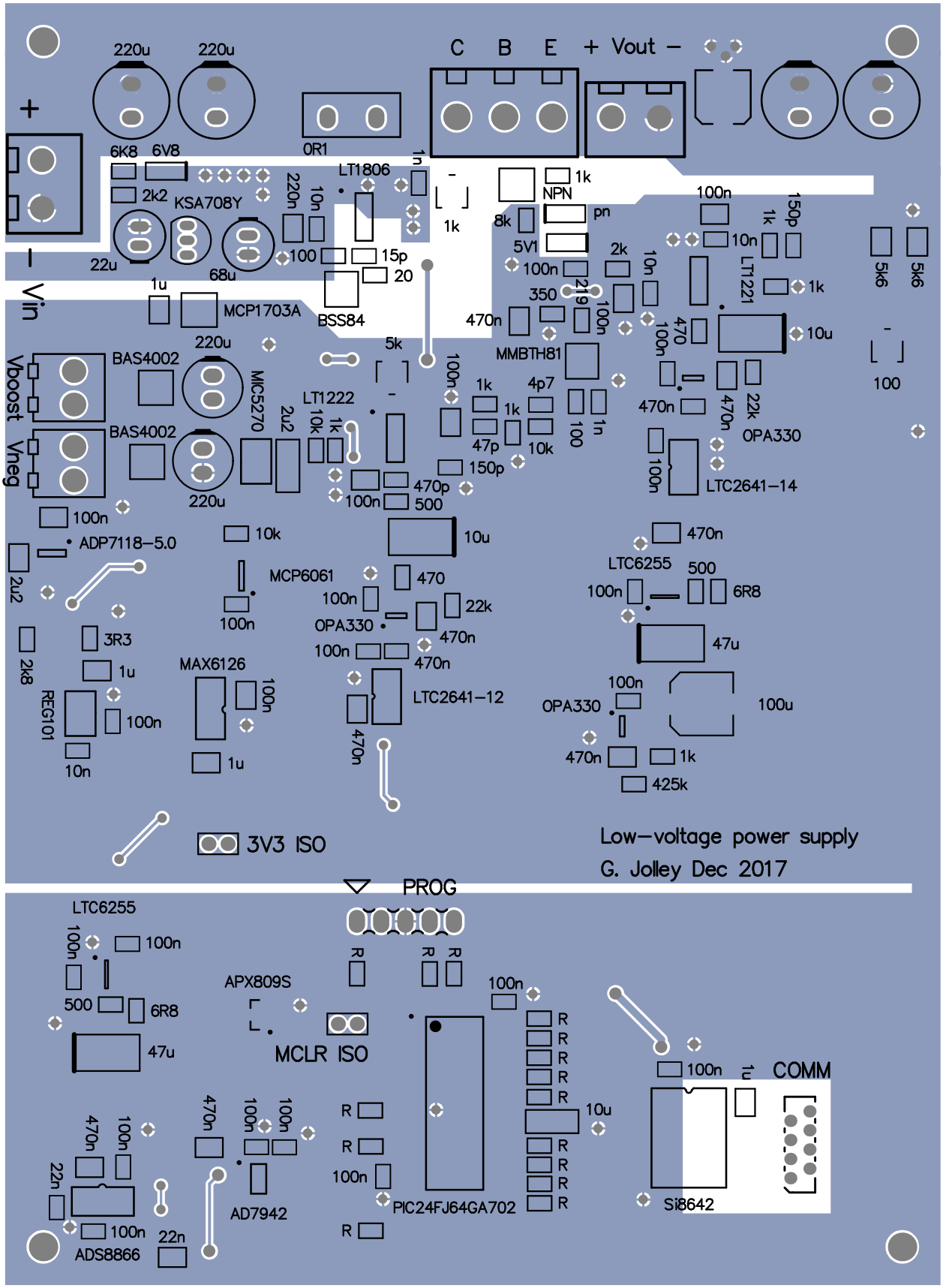

Figure 39: Low-voltage PCB bottom layer.

6.3 Control board

The control board consists of a PIC24FJ64GA704 microctroller, SPI clock buffers with output enable and interface connectors.

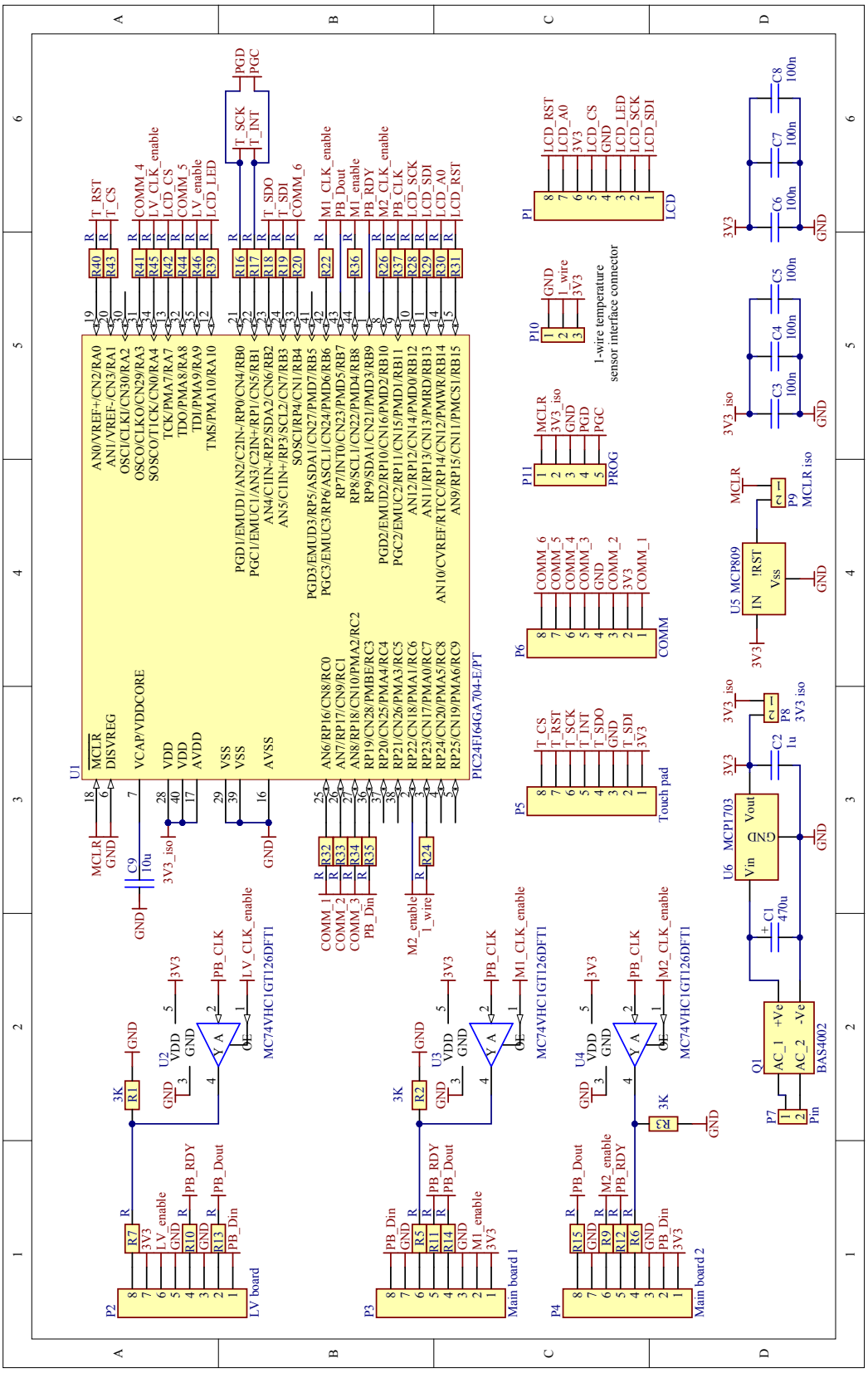

Figure 40: Control board schematic diagram.

6.4 Touchpad and LCD

A touchpad based on an LC717A10AJ capacitive sensor was designed for the user input. For prototyping and single unit project runs, user keyboard input based on capacitive sensing allows for customisation of key layout and labelling when compared with off-the-shelf mechanical keyboards. Having said that, the keyboard I designed looks very standard mostly because I had not made any firm decision on how the user interface would look before I designed it. My experience with the LC717A10AJ began with this power supply project and has been very positive in terms of sensitivity and noise immunity. A 128×64 resolution LCD, model, NHD-C12864LZ-FSW-FBW-3V3 serves as the display output.

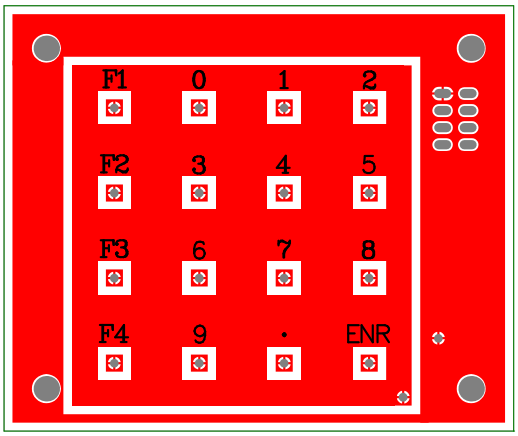

Figure 41: Touchpad PCB top layer.

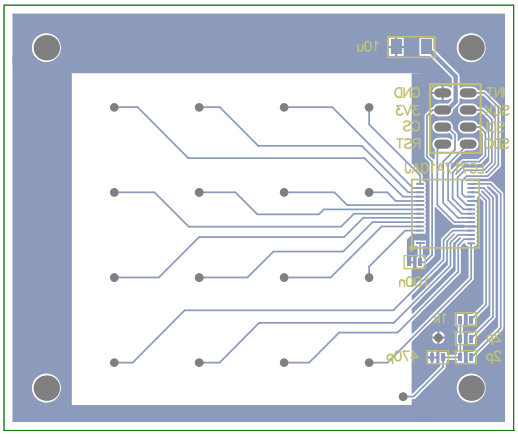

Figure 42: Touchpad PCB bottom layer.

7 Final Characterisation

All power boards and the control board were programmed with basic initial versions of software and connected together. The initial software allowed for voltage and current limit setting for characterisation, along with readout of the supply parameters. Characterisation of the final supply follows the methods used for the prototype board, apart from the use of transformers for evaluation of the ripple voltage. The output ripple of the main power boards was found to be several time greater than expected. The issue was traced to the current ripple flowing through C41, a 220 μF capacitor at the top left side of the board. This ripple current flows through the ground plane and puts the reference voltage circuitry at a slightly different ground potential than the supply output. A Cu wire (AWG 16) soldered on the reverse side of the PCB between the ground connection of C41 and the output capacitors reduced the output ripple significantly. Although the ripple current through C41 is moderate and the ground plane rather solid, we are talking about very small ripple voltages and these sorts of contributions are easily overlooked!

7.1 Main power board characterisation

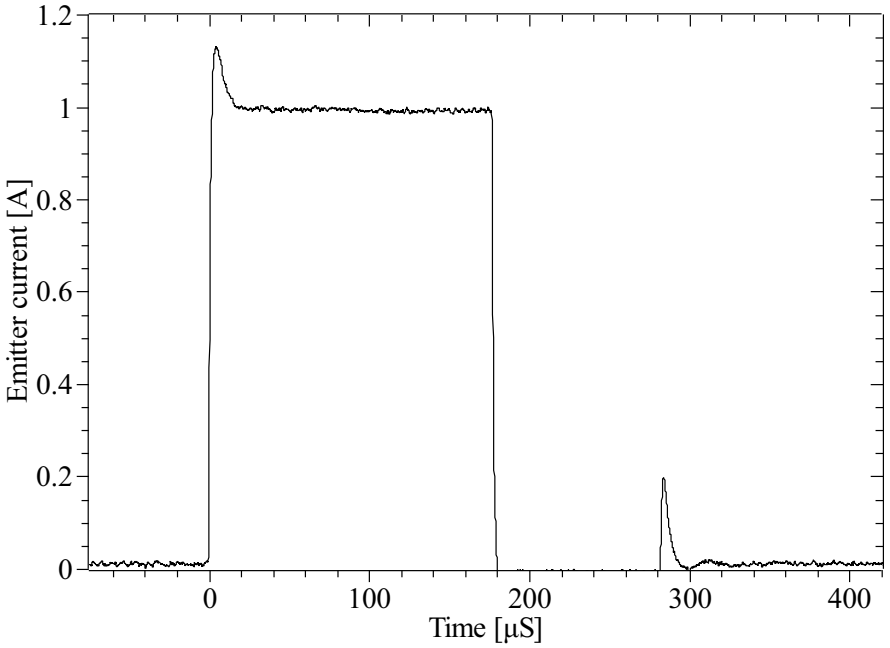

Figure 43: Main board CV characterisation.

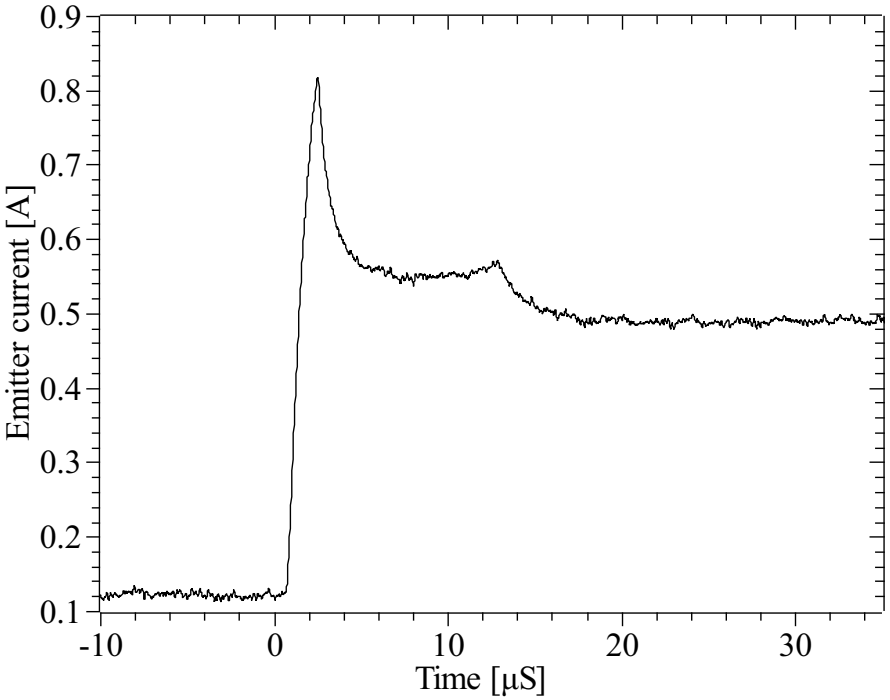

Figure 44: Main board CC characterisation.

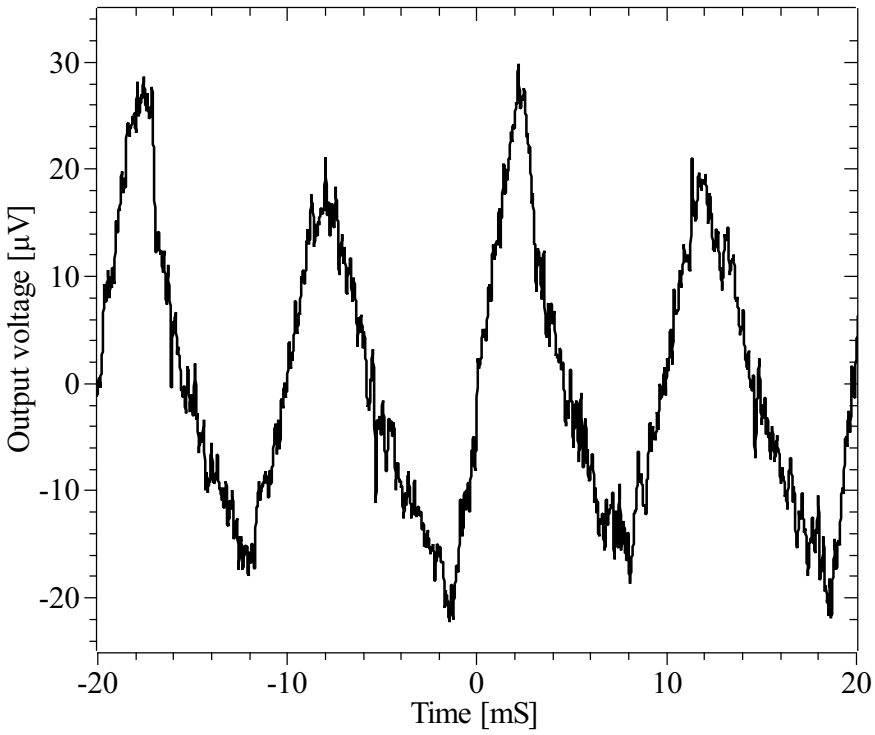

Figure 45: Main board CV ripple for a load current of 1A.

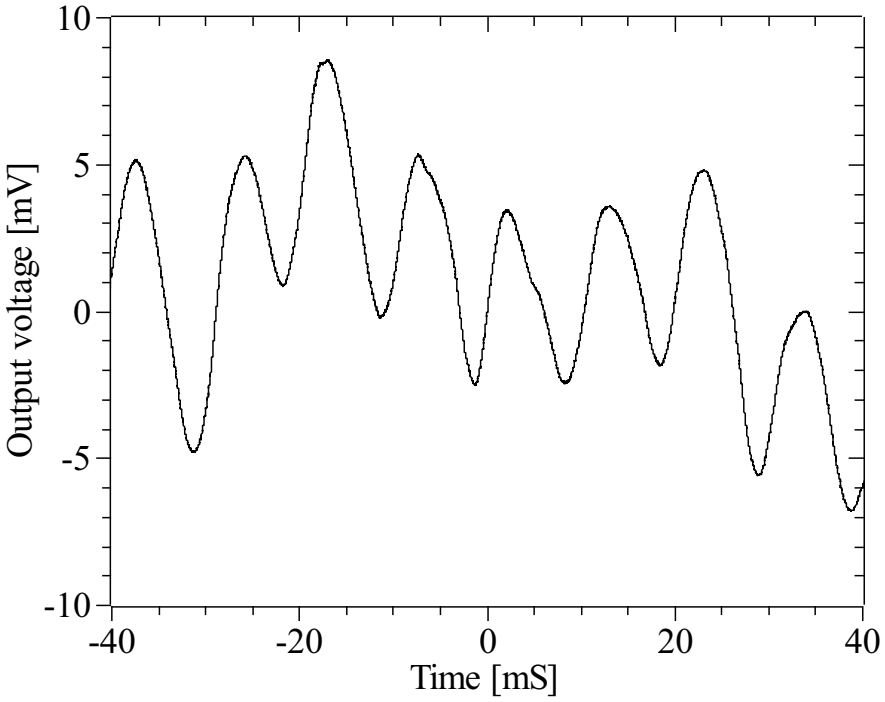

Figure 46: Main board output voltage ripple across a $8 \cdot 8\ \Omega$ load resistor with the supply in CC mode and supplying $0 \cdot 5\,\mathrm{A}$.

7.2 Low-voltage board characterisation

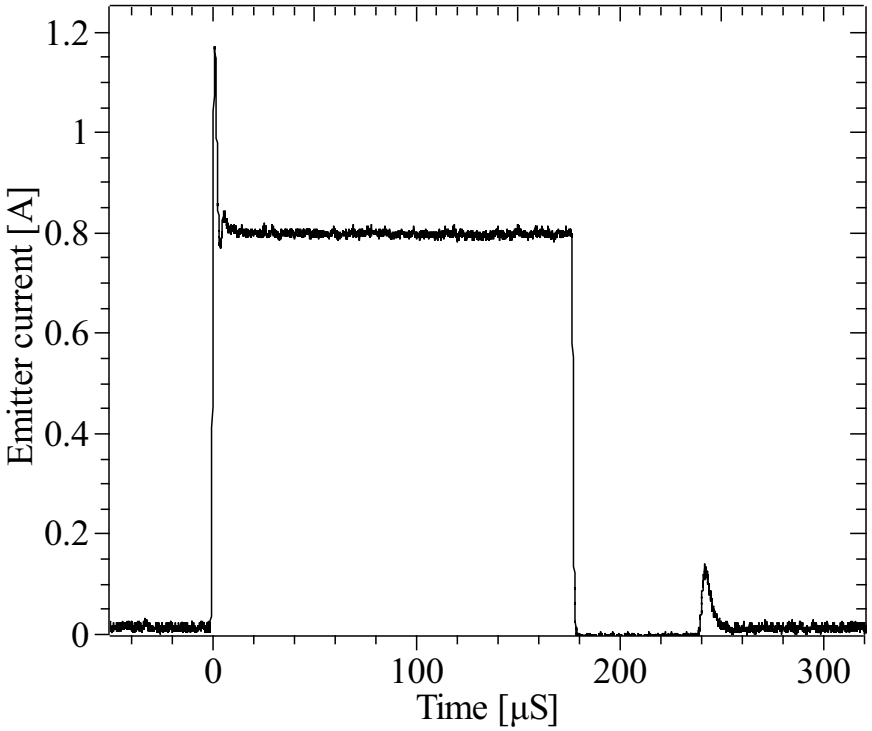

Figure 47: Low-voltage board CV characterisation.

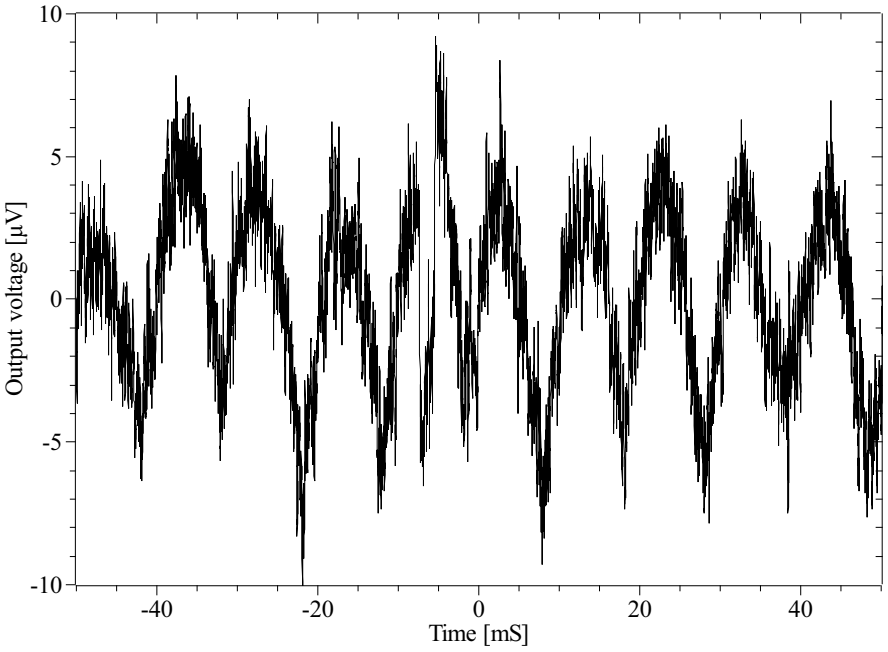

Figure 48: Low-voltage board CV ripple.

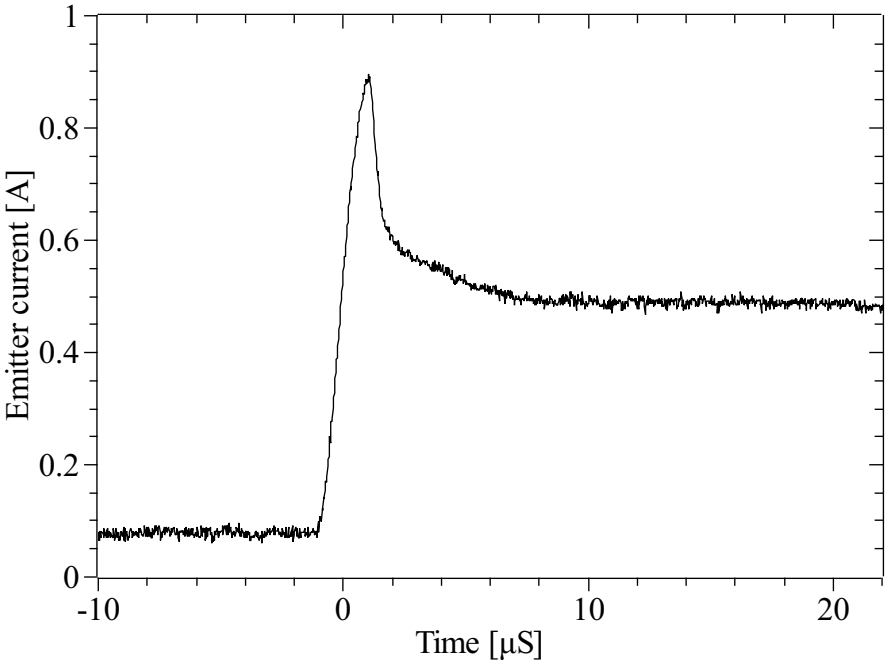

Figure 49: Low-voltage CC characterisation.

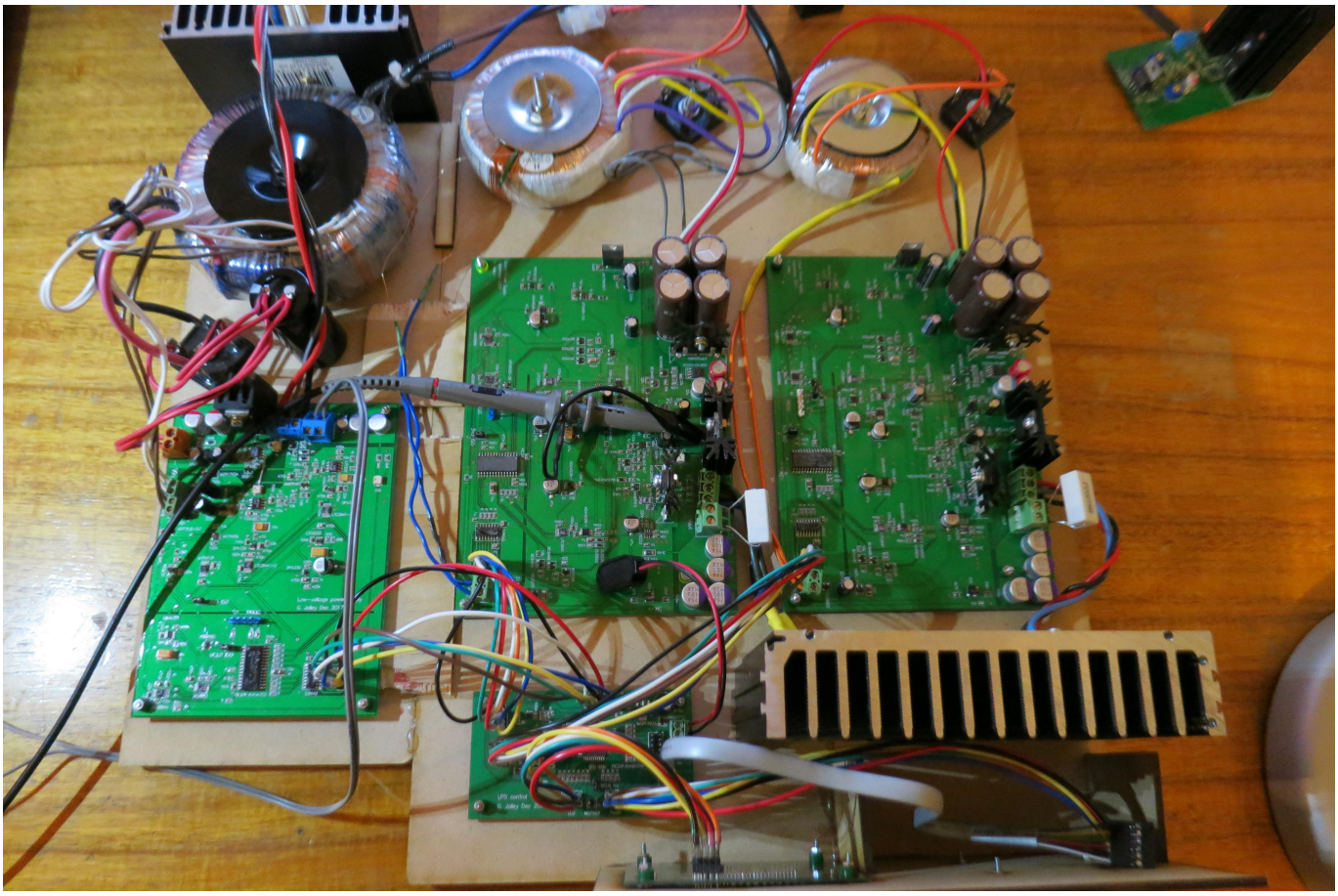

Figure 50: Constructed power, control, touchpad and LCD boards for characterisation.

Control/user interface board

The control board does the following:

- Responds to user commands
- Communicates commands to power boards
- Reads voltage and load current parameters from the power boards
- Displays power supply parameters on an LCD

There are two appropriate choices to implement user input, a capacitance touch sensor based custom keypad or a display with touch sensing. It has been decided that a capacitance touch sensing keypad will be used.

- Communicate with 3 power boards
- Communicate with touch sensor
- Communicate with LCD
- Temperature sensors
- Backlight

Program structure

All communication between the control and power boards occur via microcontroller incorporated SPI ports. All SPI ports have a transmit and receive FIFO which is configured to a 16-bit width and is 8 words deep. The control board SPI port is configured as master and initiates all communication. The control board communicates with a specific power board by asserting corresponding CLK enable and digital isolator enable signals. The control board then loads its SPI port TX buffer with a 16-bit word upon which the CLK signal undergoes 16 cycles and the 16-bit word is transferred to the power board RX FIFO buffer. Note, during this process a dummy word preloaded into the power board TX buffer is transferred to the control board and discarded. The initial word transmitted to the power board is interpreted as an instruction of which there are two classes, those that request to transmit data to the power board, and those that request data from the power board. If data is requested from the power board it loads its TX buffer with the necessary data and subsequently asserts its RDY signal. The control board, upon determining that the RDY signal is asserted, loads dummy words into its TX buffer and receives the data from the power board. When the power board determines that there are no pending transmissions it clears its RDY signal and the control board program moves onto its next communications sequence or other tasks.

The control board asserts a clk enable signal corresponding to a specific power board and sends a 16-bit word to its SPI port. The power board interprets the 16-bit word as an instruction and loads its 8-word deep FIFO SPI transmit buffer with data, if the control board is reading data from the power board, or dummy data if the control board is writing data to the power board. The power board then asserts a ready signal. The control board subsequently clocks data to or from the power board. The power board determines when the control board has transmitted or received all data corresponding to the initial instruction sent and clears the ready signal such that the control board program can progress to its next task.

- The power boards load a dummy word in the SPI
- The control board asserts the CLK enable and ISO enable signals
- The control boards sends an instruction to the power board
- The power board monitors its receive buffer status and when it has determined that a 16-bit word has been transferred it decodes the word and if a valid instruction has been received it loads either dummy data (if the control board is sending data) or data (if the control board is reading data)
- Upon loading the data to send to the control board the power board asserts its RDY signal
- Upon determining that the RDY signal is asserted the control board initiates SPI transfers
- Upon receiving or sending data to the control board, and acting upon any received data the power board clears its RDY signal

- Only when the control board determines that the RDY signal is clear does it move on to subsequent tasks

The following possible conditions will derail communications:

- The control board sends an instruction to a power board that does not have a dummy word loaded into its buffer

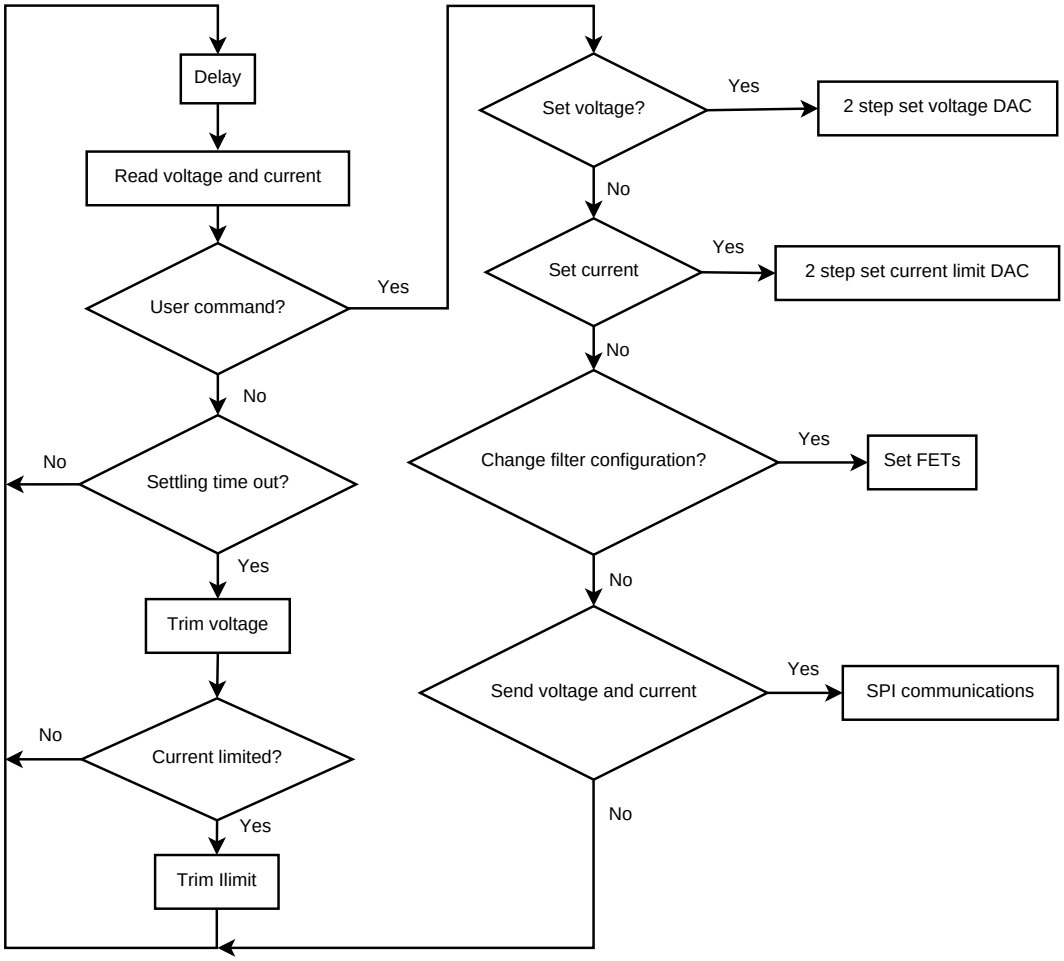

Figure 51: Flowchart of the main board MCU program.